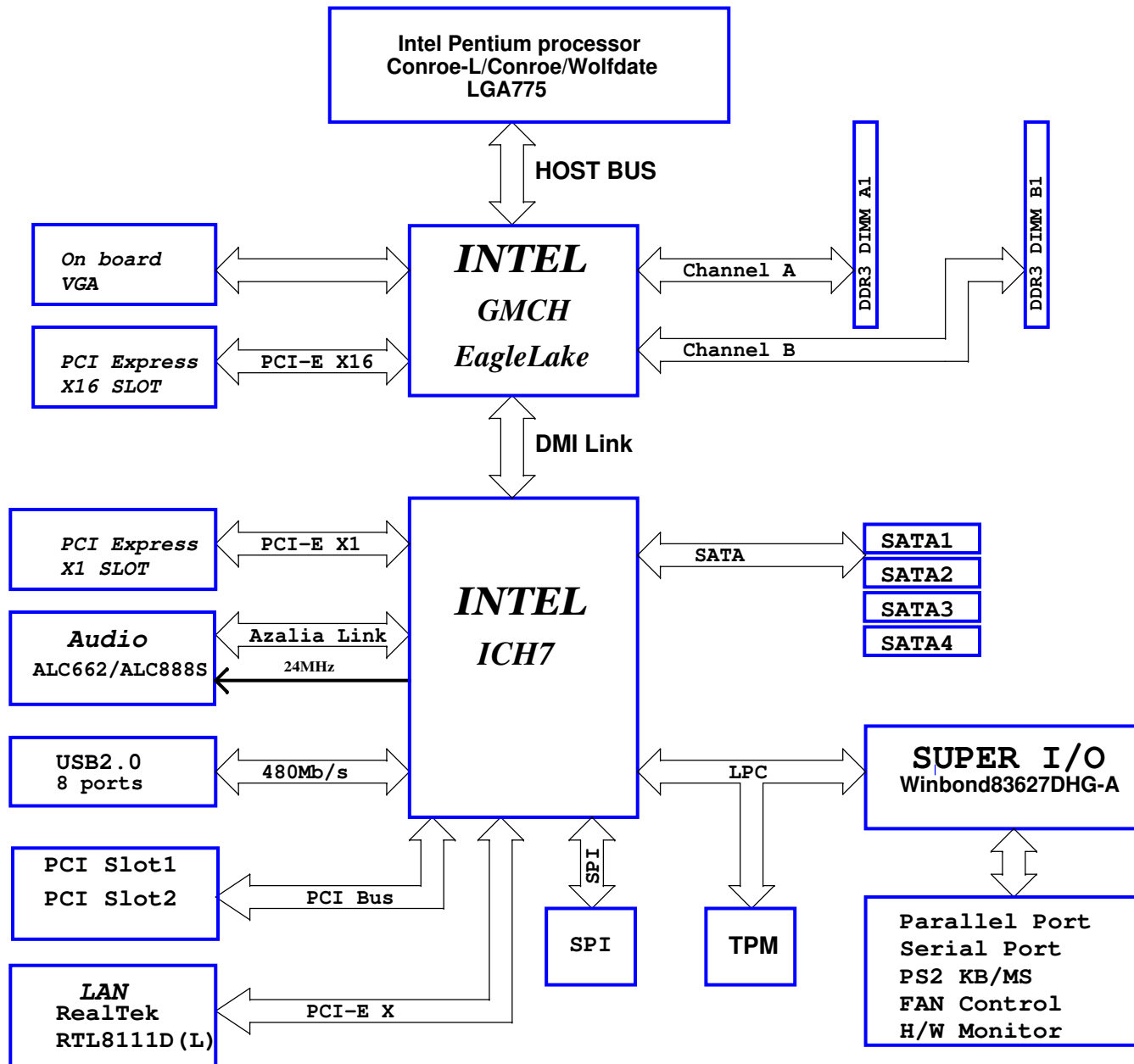


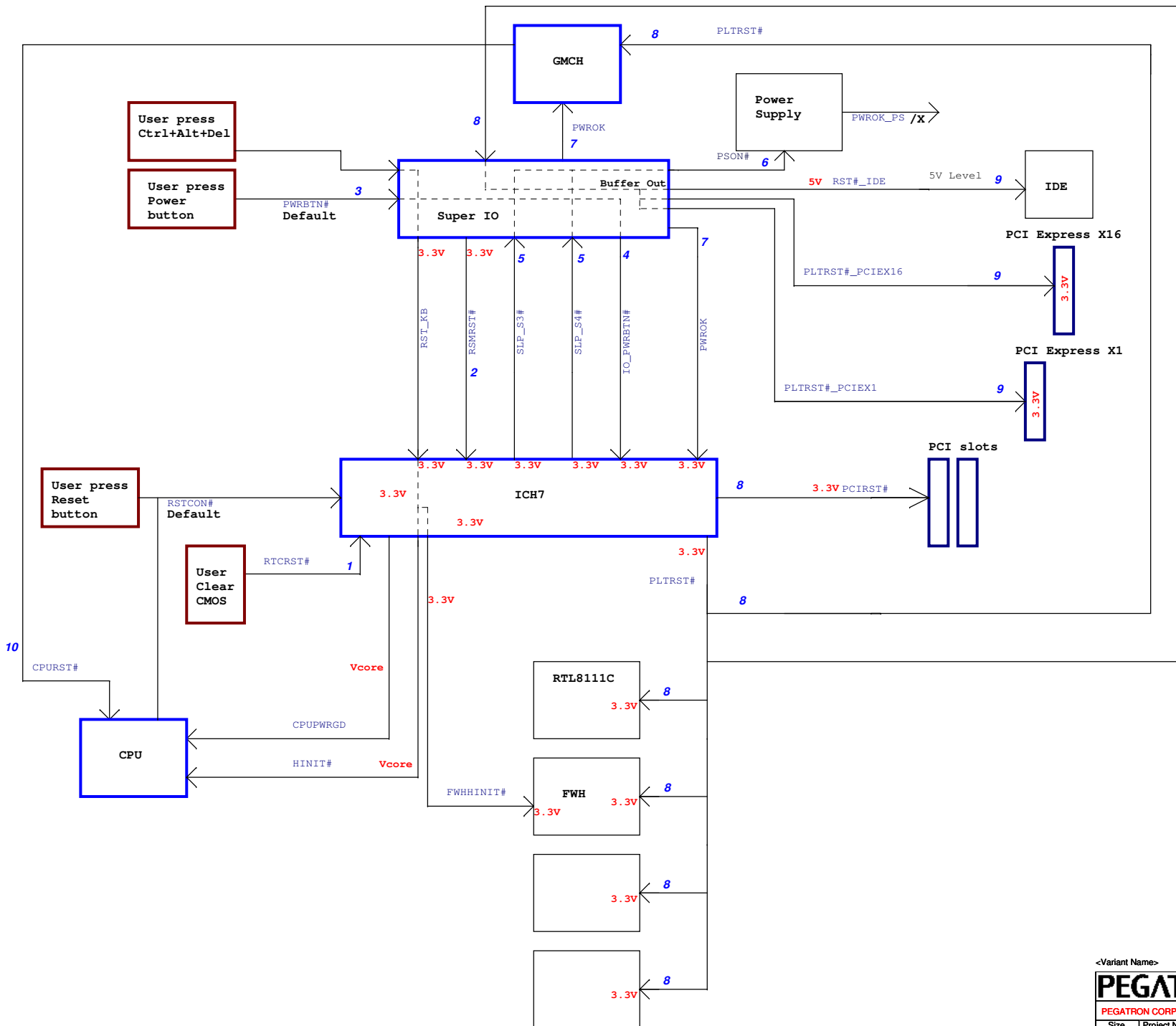
IPM41-D3

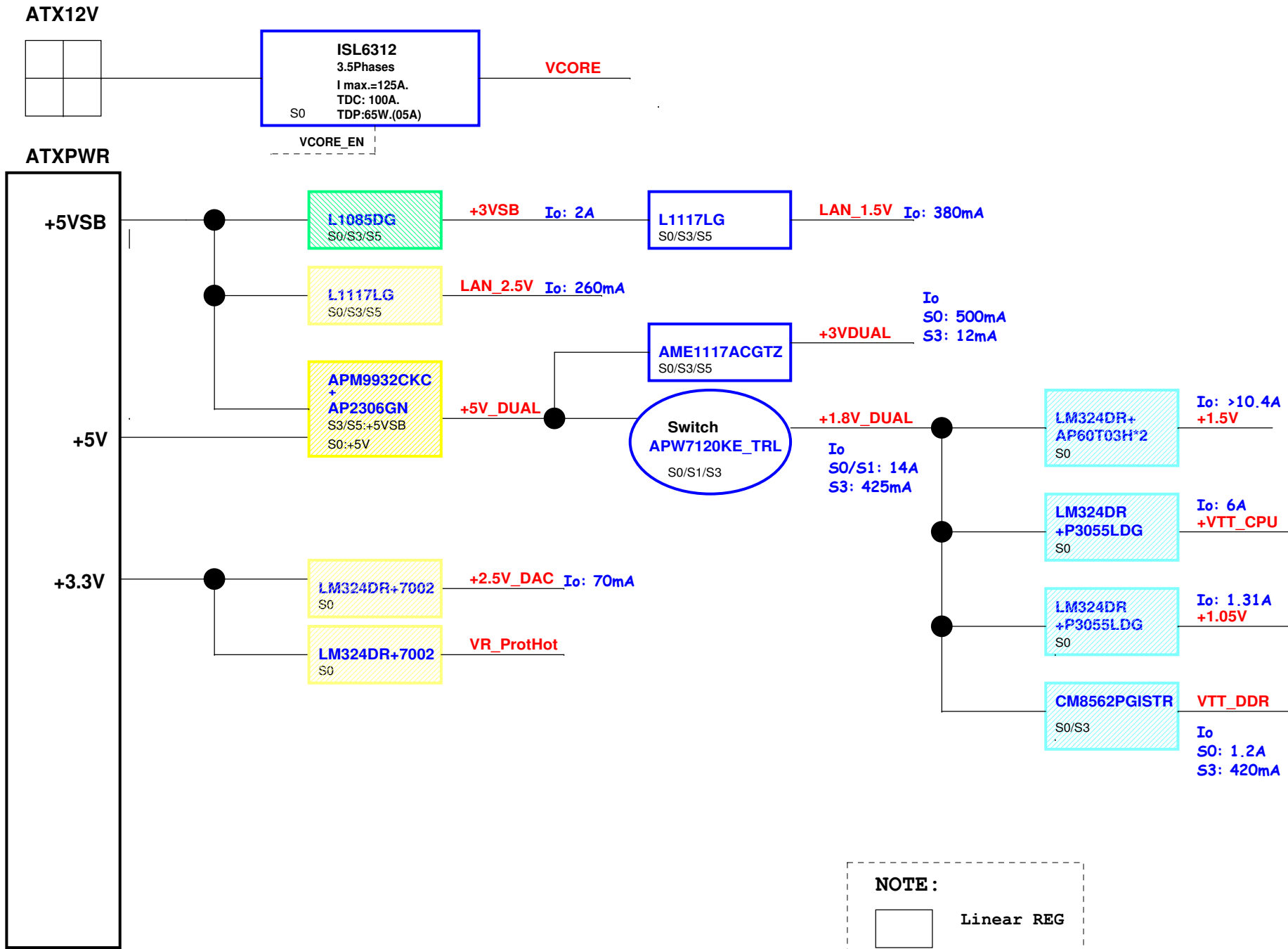
Revision:1.00

53	+1P1V_CORE
54	SPI 4Mb
55	RTC / CMOS / SPKR/SCREW HOLE



01	Block Diagram
02	Power Sequence
03	Power Flow
04	Clock Distribution
05	Clock
06	PROCESSOR LGA775 1 - 3
07	PROCESSOR LGA775 2 - 3
08	PROCESSOR LGA775 3 - 3
09	ITP 31P DEBUG CONNECTOR
10	INTEL EAGLELAKE 1 - 7
11	INTEL EAGLELAKE 2 - 7
12	INTEL EAGLELAKE 3 - 7
13	INTEL EAGLELAKE 4 - 7
14	INTEL EAGLELAKE 5 - 7
15	INTEL EAGLELAKE 6 - 7
16	INTEL EAGLELAKE 7 - 7
17	DDR2 CHANNEL A
18	DDR2 CHANNEL B
19	DDR2 TERMINATION A&B
20	ICH7-1
21	ICH7-2
22	ICH7-3
23	ICH7-4
24	PCI EXPRESS X16 SLOT
25	PCI EXPRESS X1 SLOT
26	INTEGRATED VGA PORT
27	SATA CONNECTORS
28	PCI SLOT INTERFACE - PCI1
29	PCI SLOT INTERFACE - PCI2
30	DOUBLE STACK PORT CONNECTOR
31	USB HEADER CONNECTOR
32	REALTEK RTL8111C CONTROLLER
33	RJ-45+USB CONNECTOR
34	ALC662/883
35	AUDIO Connector
36	FRONT AUDIO CONNECTOR
37	TPM HEADER INTERFACE
38	SUPER I/O W83627DHG - 1 OF 2
39	SUPER I/O W83627DHG - 2 OF 2
40	PARALLEL PORT - CPC
41	SERIAL PORT CONNECTOR- SI
42	PS2 KB &MS CONNECTOR FOR CPC
43	FAN CIRCUIT FOR 4 - PIN
44	FRONT PANEL CIRCUIT FOR CPC
45	ATX POWER 24P CONNECTOR
46	VCORE CONTROLLER - RT8857
47	VCORE DRIVER - RT9619_1
48	VCORE DRIVER - RT9619_2
49	+0P9V_VTT_DDR_LDO
50	+1P1V_FSB_VTT&+5V_DUAL
51	PSI CIRCUIT
52	+1P8V_DUAL





NOTE:



Linear REG



Switch REG

<Variant Name>

PEGATRON		Title : Power Flow	
PEGATRON CORP.		Engineer: Wayne Hsieh	
Size A3	Project Name IPM41-D3	Rev 1.00G	
Date: Thursday, July 09, 2009		Sheet 3 of 55	

XTAL

14.318 MHz

ICS
9LPRS552AGLF_T

133/200/266 MHz

CK_FSB_CPU/#

CPU

133/200/266 MHz

CK_FSB_NB/#

MCH

Lakeport

100 MHz

CK_100M_MCH/#

96 MHz

CK_96M_DREF/#

100 MHz

CK_100M_PCIEX16/#

PCIEX16

100 MHz

CK_100M_ICH/#

ICH7

100 MHz

CK_100M_SATA/#

48 MHz

CK_48M_USB

33 MHz

CK_33M_ICH

14.318 MHz

CK_14M_ICH

48 MHz

CK_48M_SIO

Super I/O

33 MHz

CK_33M_SIO

33 MHz

33 MHz

CK_PCI_TPM

TCM

33 MHz

CK_33M_SL1

PCI SLOT 1

33 MHz

CK_33M_SL2

PCI SLOT 2

100 MHz

CK_PCIE_SLOT1/#

PCIEX1_1

100 MHz

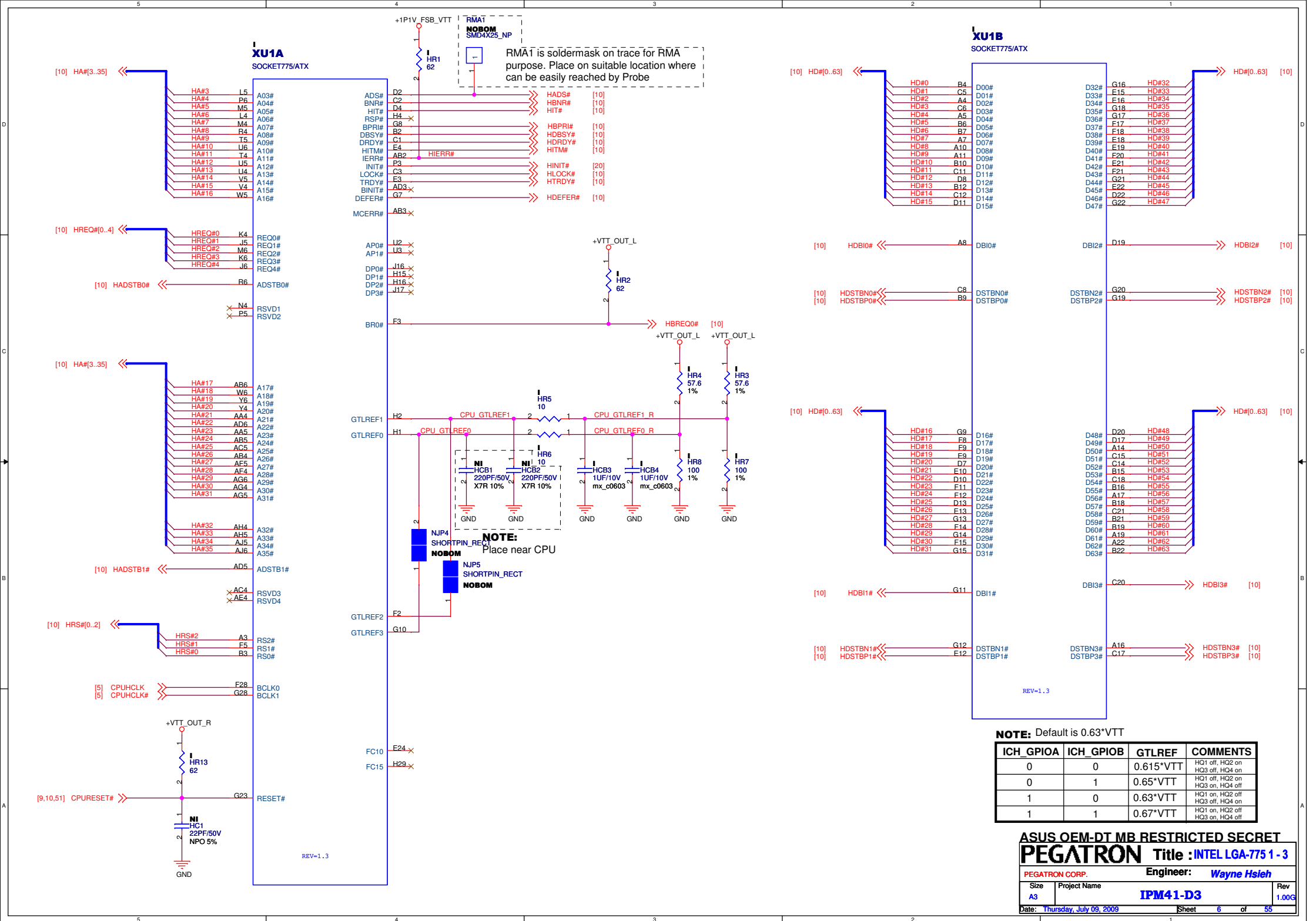
CK_100M_LAN/#

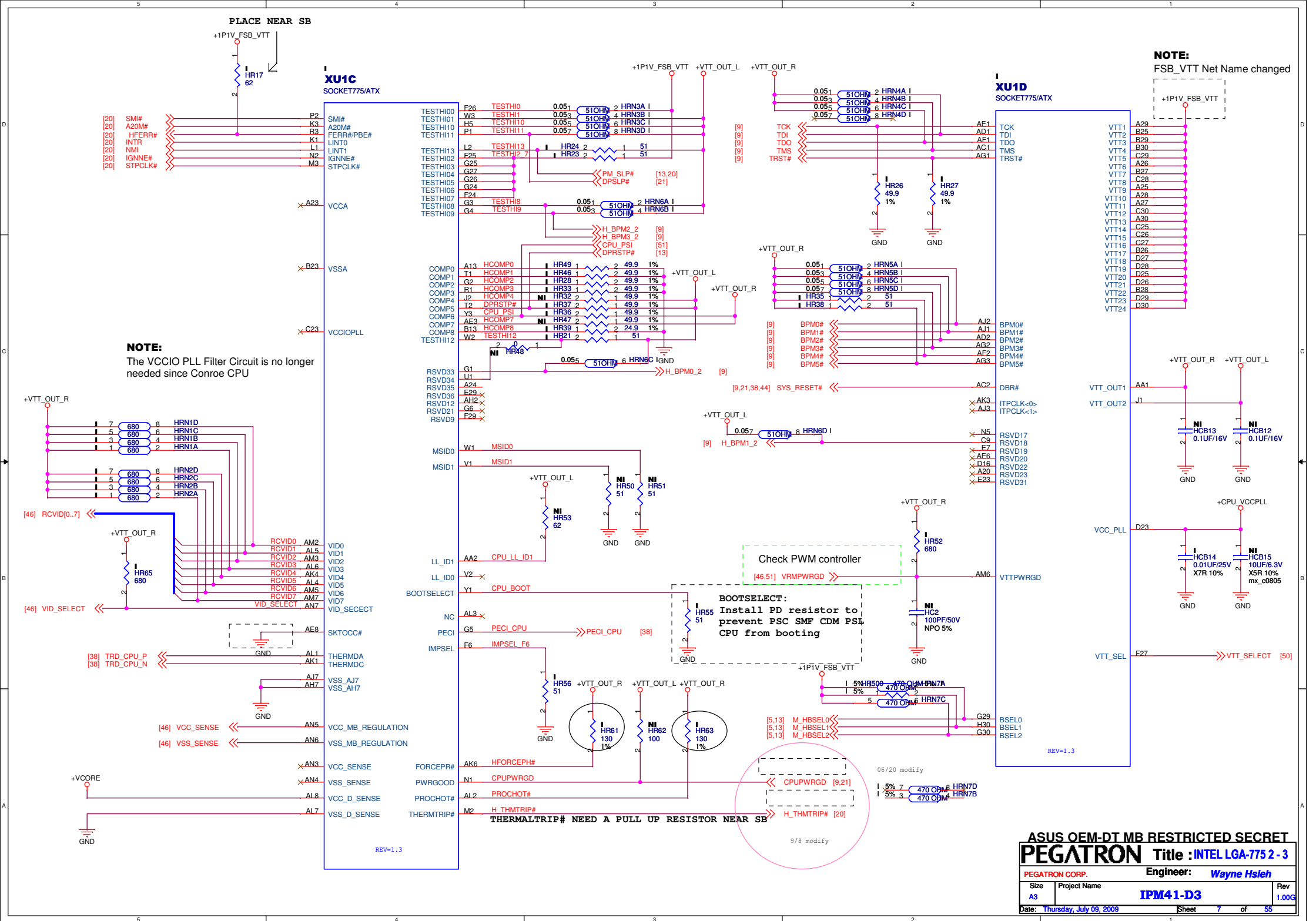
LAN

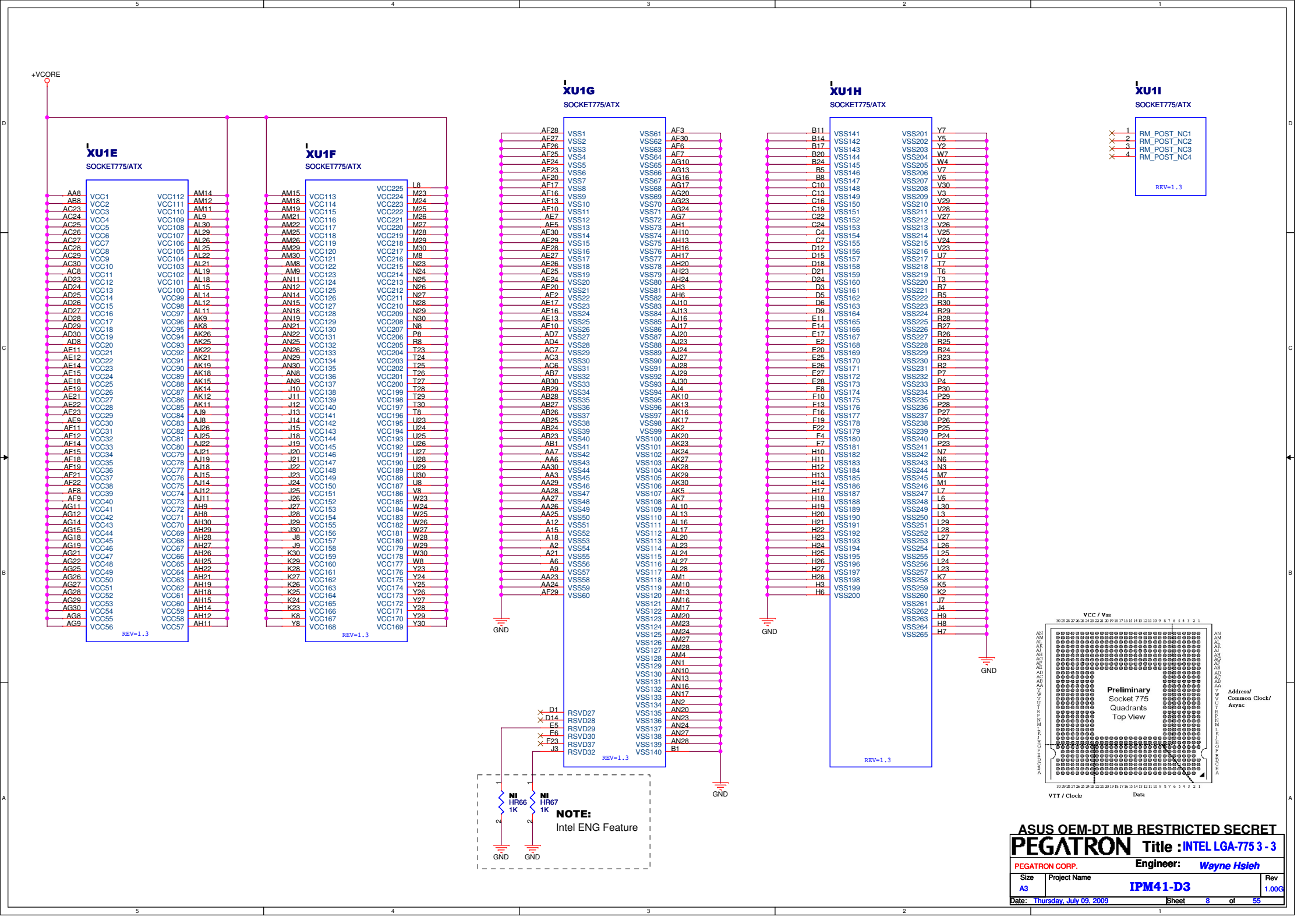
<Variant Name>

PEGATRON		Title : Clock Distribution	
PEGATRON CORP.		Engineer: Wayne Hsieh	
Size A3	Project Name IPM41-D3		Rev 0.00G
Date: Thursday, July 09, 2009		Sheet 4 of 55	

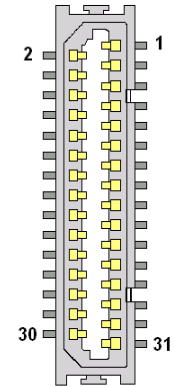
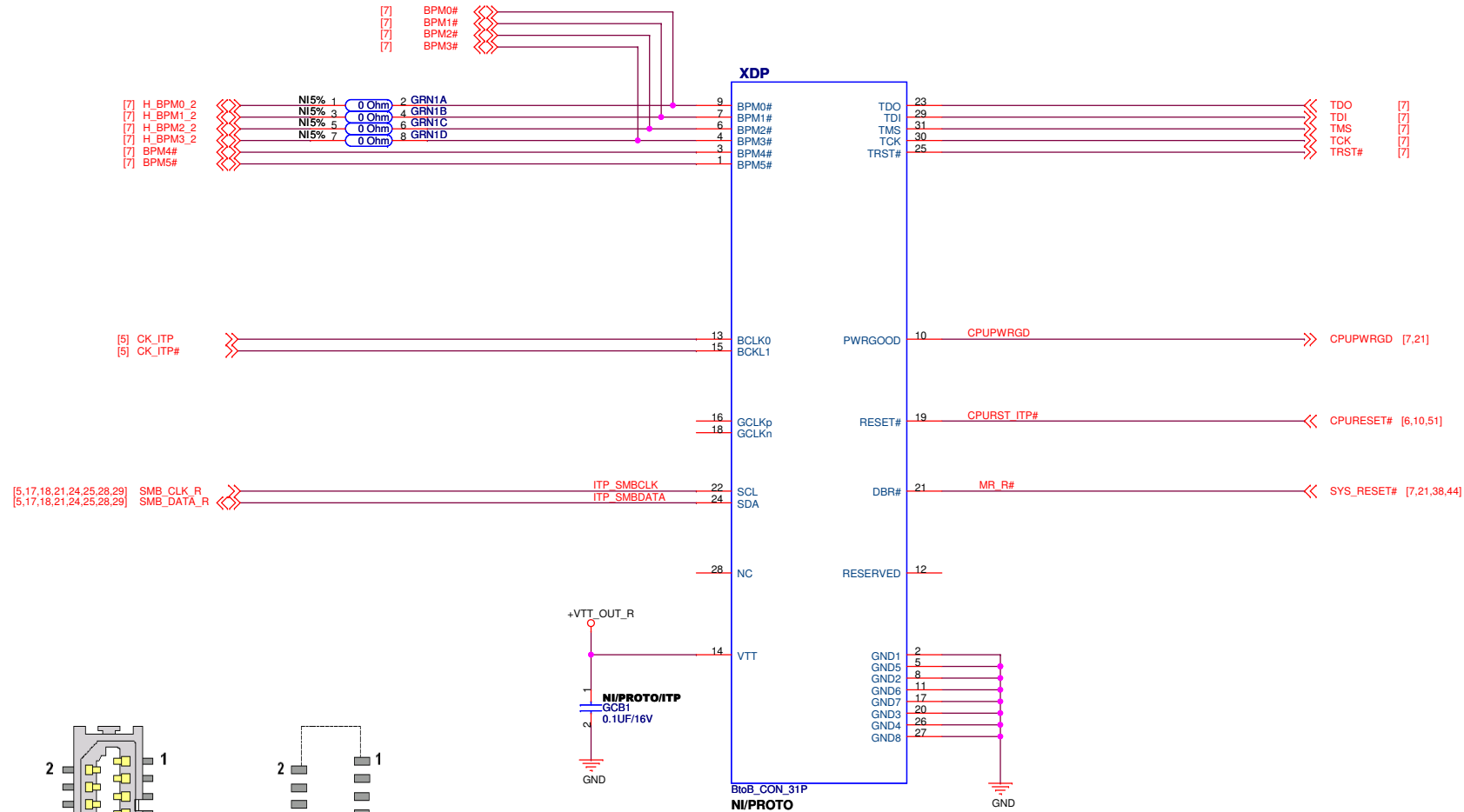




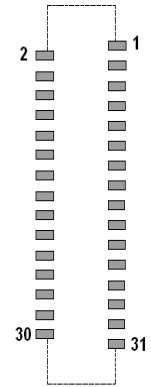




INTEL LGA-775 PROCESSOR ITP DEBUG PORT



HRS/DF9C-31S-1V(22)
TOP SIDE VIEW



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT

PEGATRON P/N: 12X64A531W00

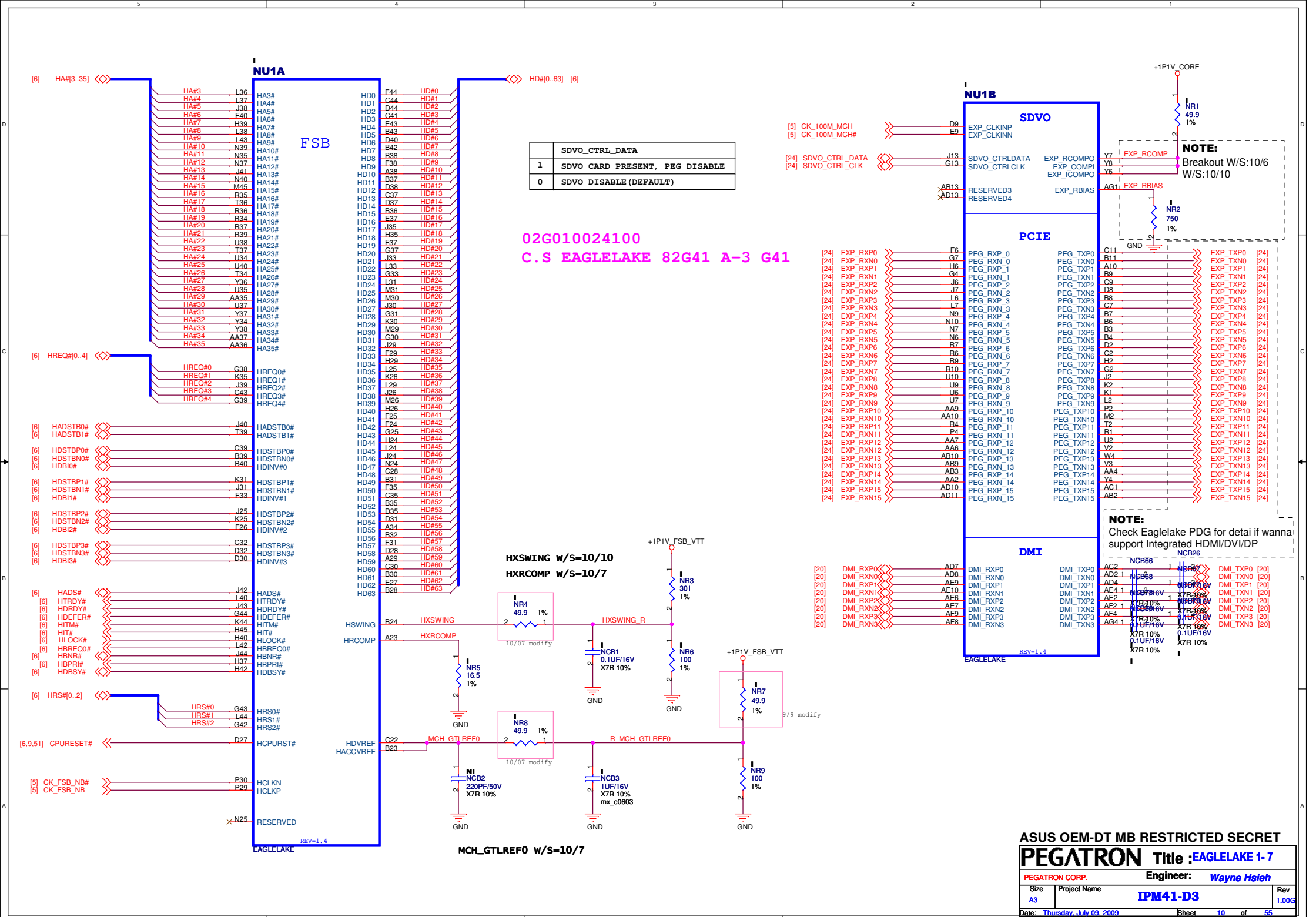
ASUS OEM-DT MB RESTRICTED SECRET

ASUS Title : ITP_31P CONN.

PEGATRON CORP. Engineer: Wayne Hsieh

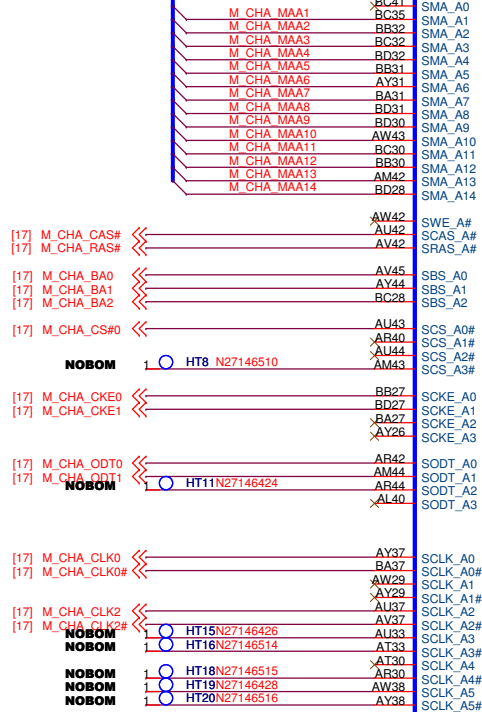
Size A3 Project Name IPM41-D3 Rev 1.00G

Date: Thursday, April 29, 2010 Sheet 9 of 55

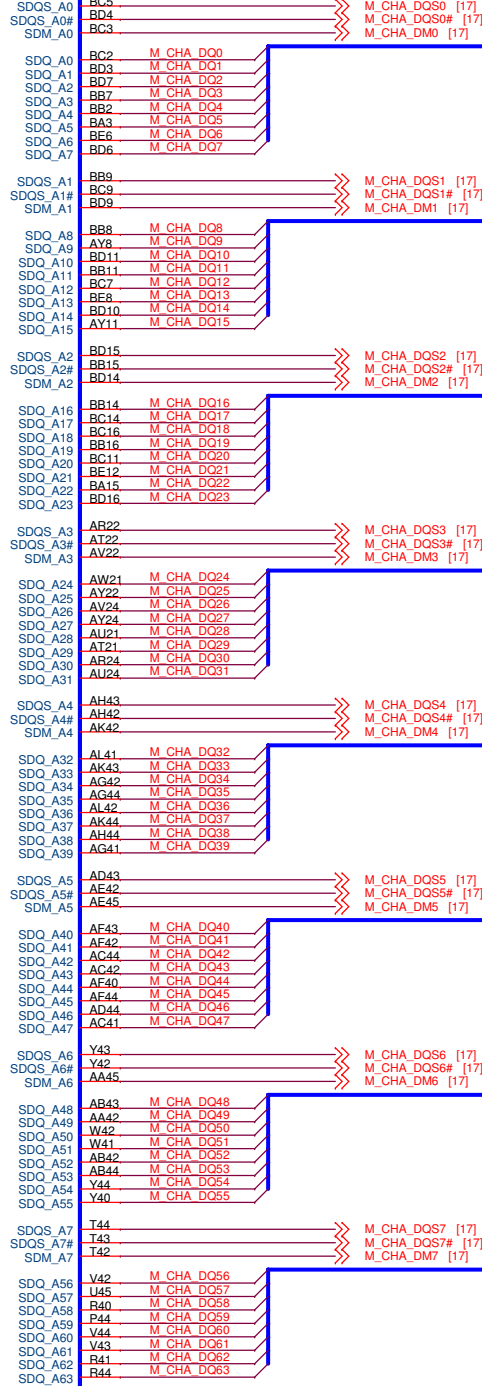


[17] M_CHA_MAA[1..14] <<

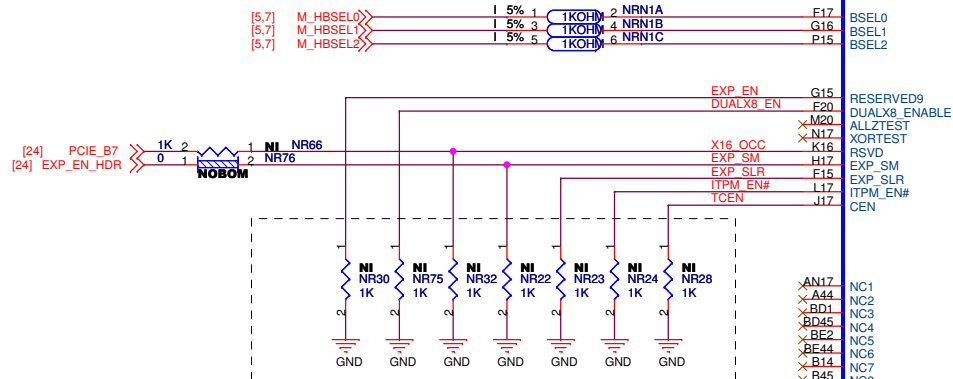
NU1C



DDR_A

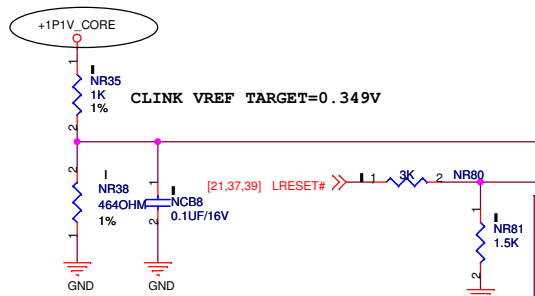


M_CHA_DQ[0..63] [17]



NOTE:

PIN	HIGH	LOW	DESCRIPTION
EXP_SM	CONCURRENT	NOT CONCURRENT	PCI-E/SDVO
DUALX8	1x16 PCIe	2x8 PCIe	DUALX8 ENABLE
X16_OCC	NOT PRESENCE	PRESENCE	PCIe CARD IN PRIMARY SLOT
EXP_SLR	NORMAL	RESERVE	PCI-E LANE RESERVAI
ITPM_EN#	DISABLE	ENABLE	iTPM Enable
TCEN	ENABLE	DISABLE	TLS CONFIDENTIALITY



- NU1E**
- RESERVED9
 - DUALX8_ENABLE
 - ALLZTEST
 - XORTEST
 - RSVD
 - EXP_SM
 - EXP_SLR
 - ITPM_EN#
 - TCEN
 - NC1
 - NC2
 - NC3
 - NC4
 - NC5
 - NC6
 - NC7
 - NC8
 - NC9
 - NC10
 - NC11
 - NC12
 - NC13
 - NC14
 - NC15
 - RESERVED10
 - BSCANTEST
 - RESERVED12
 - RESERVED13
 - RESERVED14
 - RESERVED16
 - JTAG_TDI
 - JTAG_TDO
 - JTAG_TCK
 - JTAG_TMS
 - RESERVED22
 - RESERVED23
 - RESERVED24
 - RESERVED25
 - RESERVED26
 - RESERVED27
 - RESERVED28
 - RESERVED29
 - RESERVED30
 - RESERVED32
 - RESERVED33
 - TEST0
 - TEST1
 - TEST2
 - TEST3

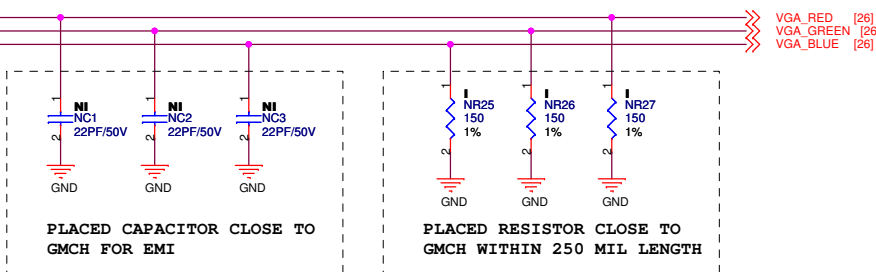
VGA



MISC



NOTE:
Install NR67 NR68 and NOT Install NR18 NR21 for non-Graphics SKU



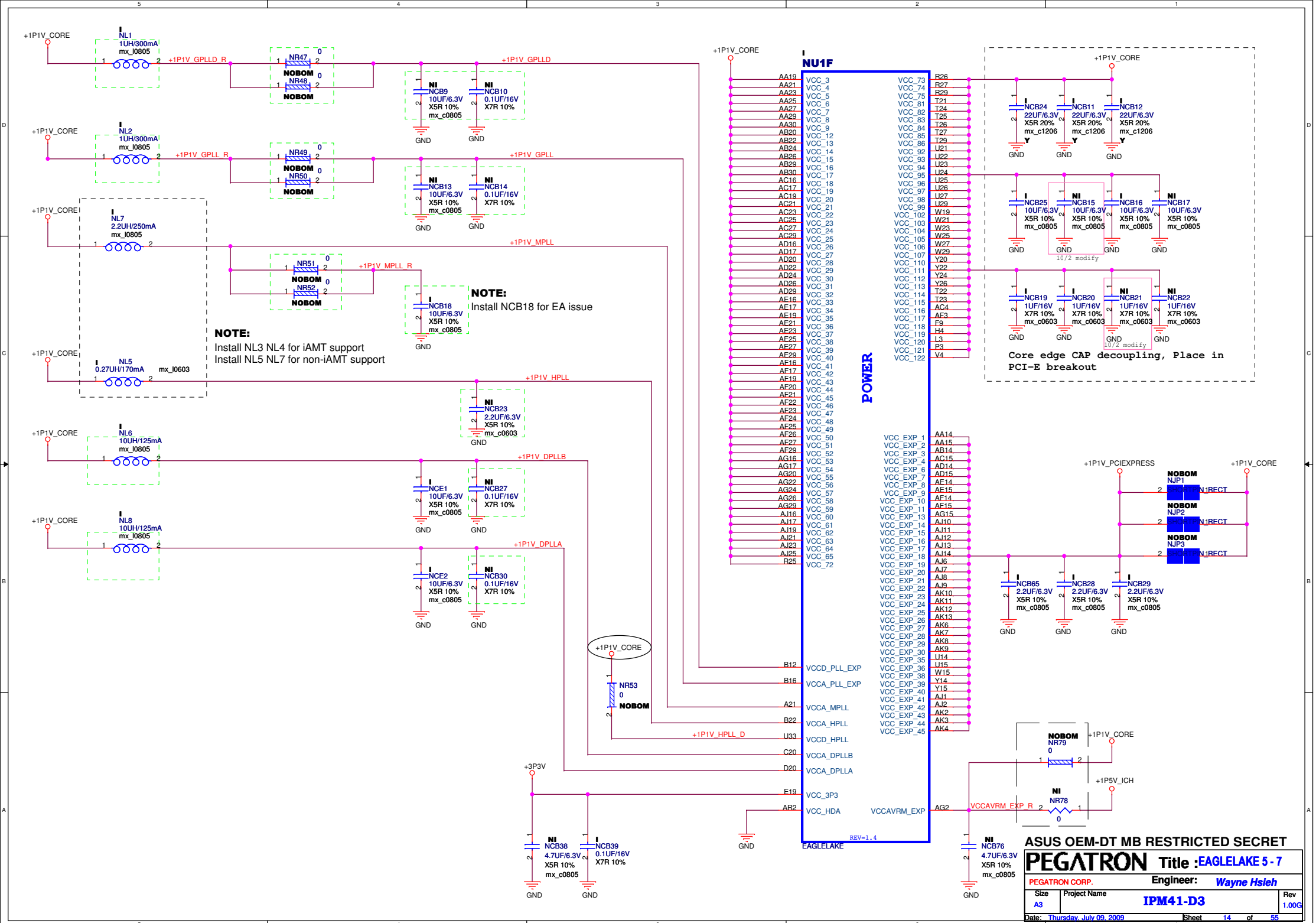
NOTE:
Change NR33 and NR25~NR27 to 0 OHM for non-Graphics SKU, KEEP PU resistor VR14~15 for DDCDATA/CLK

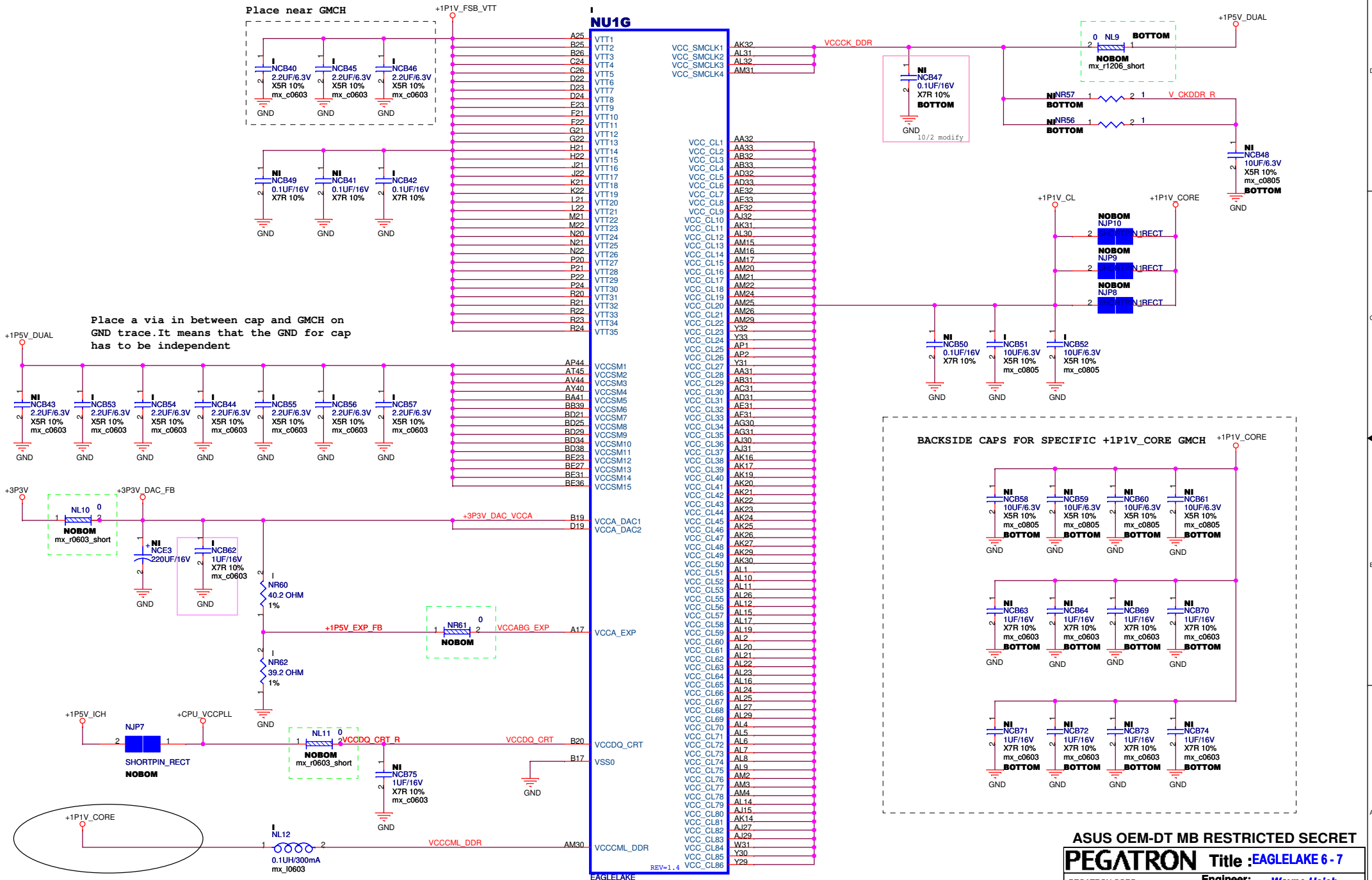


NOTE:
HDMI PORTC DDC Control CLK
HDMI PORTC DDC Control DATA

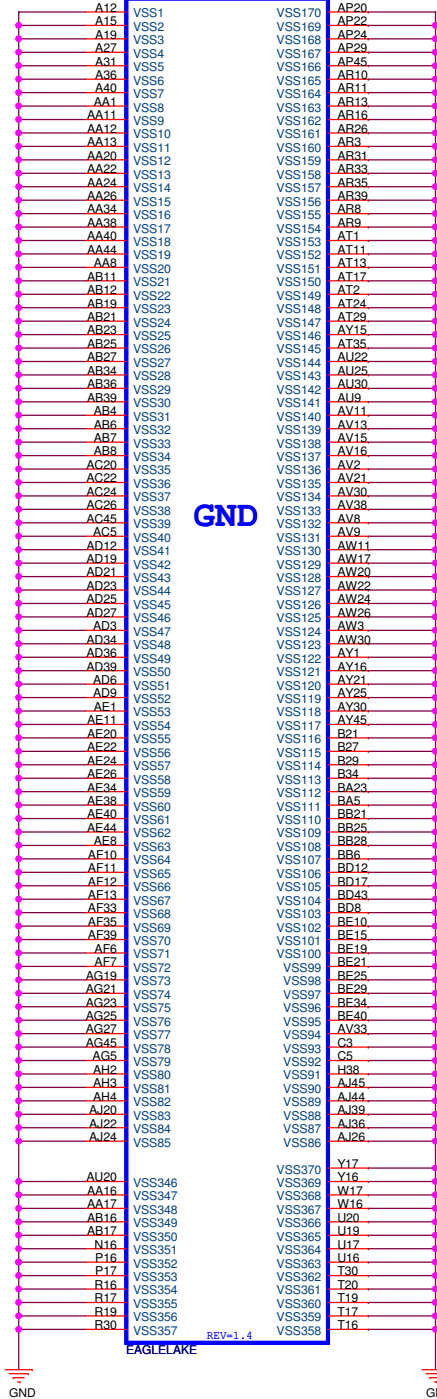


NOTE:
NR69 NR46 place near CPU side

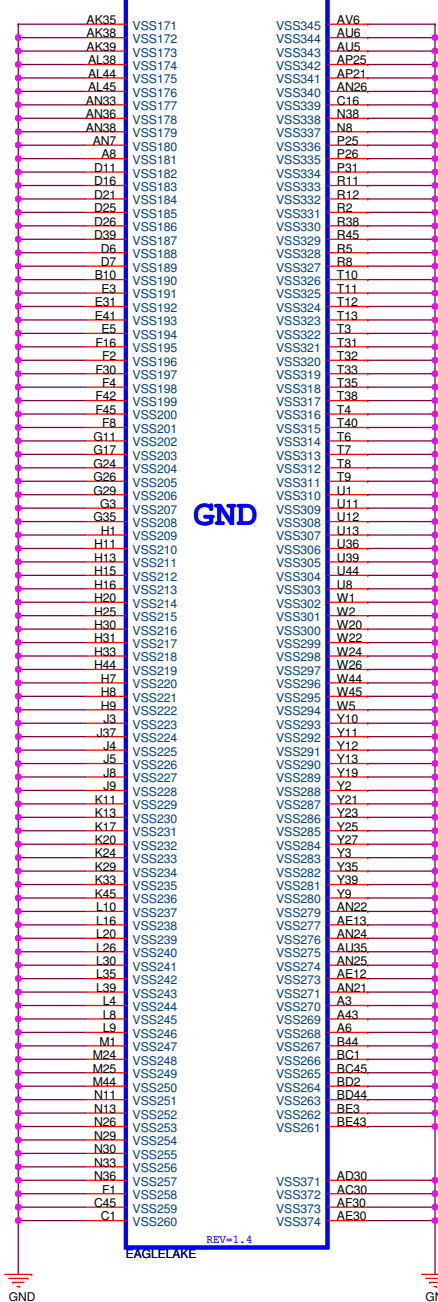




NU1H

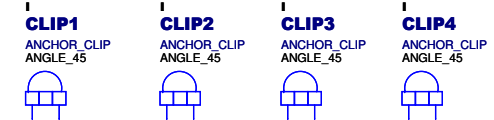
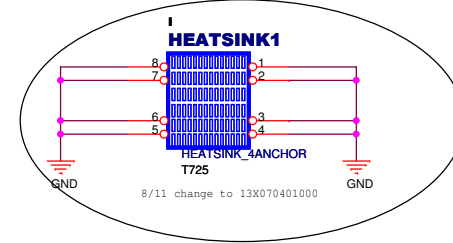


NU1I



EAGLELAKE-P/Q/G (25.2W/23.4W/25.5W)

13G070432001 HEATSINK 55.2*37.6*30MM SILVER
13G070432000 HEATSINK 55.2*37.6*30MM SILVER
13G070432002 HEATSINK 55.2*37.6*30MM SILVER



ASUS OEM-DT MB RESTRICTED SECRET

PEGATRON Title :EAGLELAKE 7 - 7

PEGATRON CORP. Engineer: Wayne Hsieh

Size A3 Project Name IPM41-D3 Rev 1.00G

Date: Thursday, July 09, 2009 Sheet 16 of 55

NOTE:
Below 4 signals are different connection in Eaglelake platform
Channel A : CS1/WE/MA0
Channel B : ODT3 (G41 No ODT3)

NOTE:

Check clock source if Eaglelake implemented

[11] M_CHA_CLK0 >> 63
[11] M_CHA_CLK1 >> 64
[11] M_CHA_CLK2 >> 184
[11] M_CHA_CLK2# >> 185
06/03 Important! follow Intel MRC code, only DIMMA need.

[12] M_CHA_CS#1 >> 76
[11] M_CHA_CS#0 >> 193
[11] M_CHA_CKE1 >> 169
[11] M_CHA_CKE0 >> 50
[11] M_CHA_BA2 >> 52
[11] M_CHA_BA1 >> 190
[11] M_CHA_BA0 >> 71

[5,9,18,21,24,25,28,29] SMB_DATA_R >> 238
[5,9,18,21,24,25,28,29] SMB_CLK_R >> 118

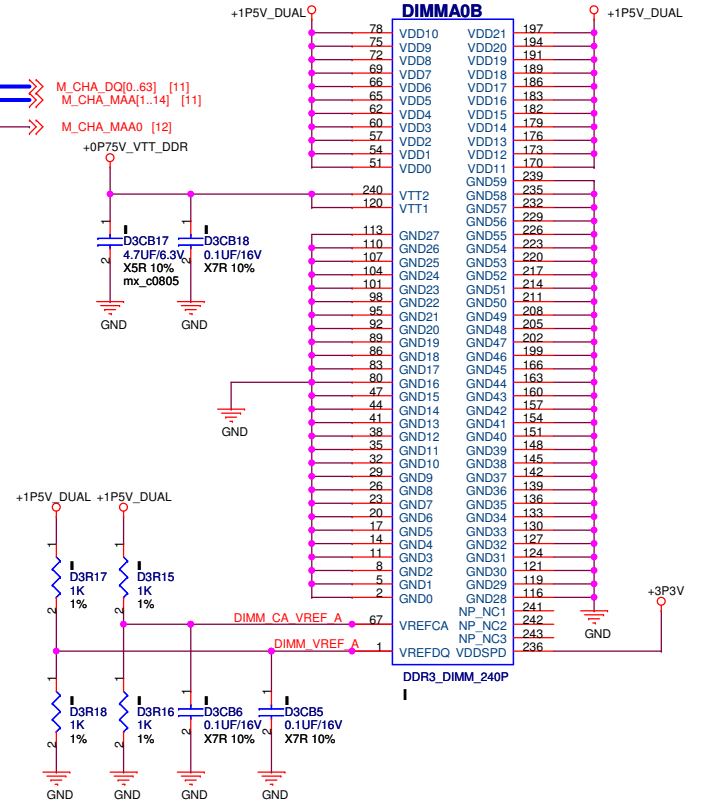
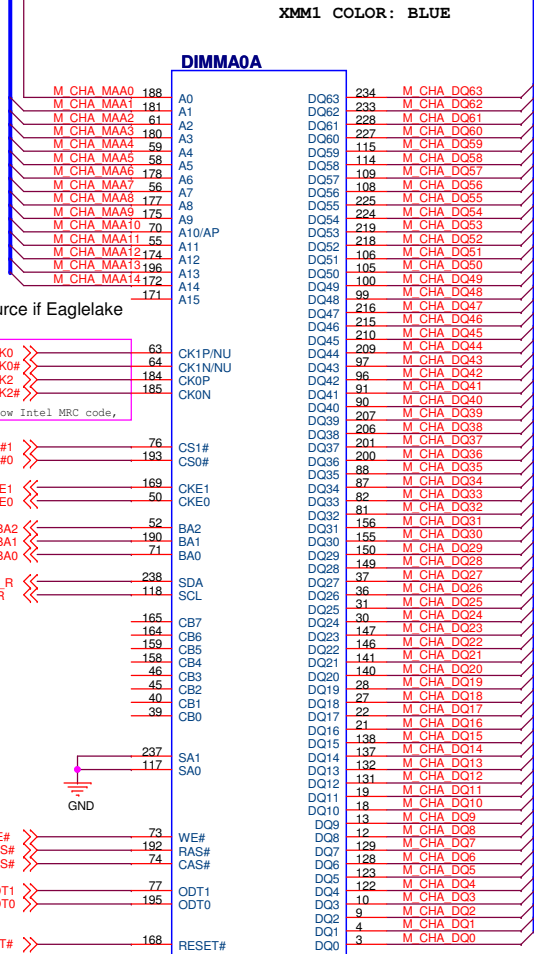
SA1 >> 237
SA0 >> 117
GND

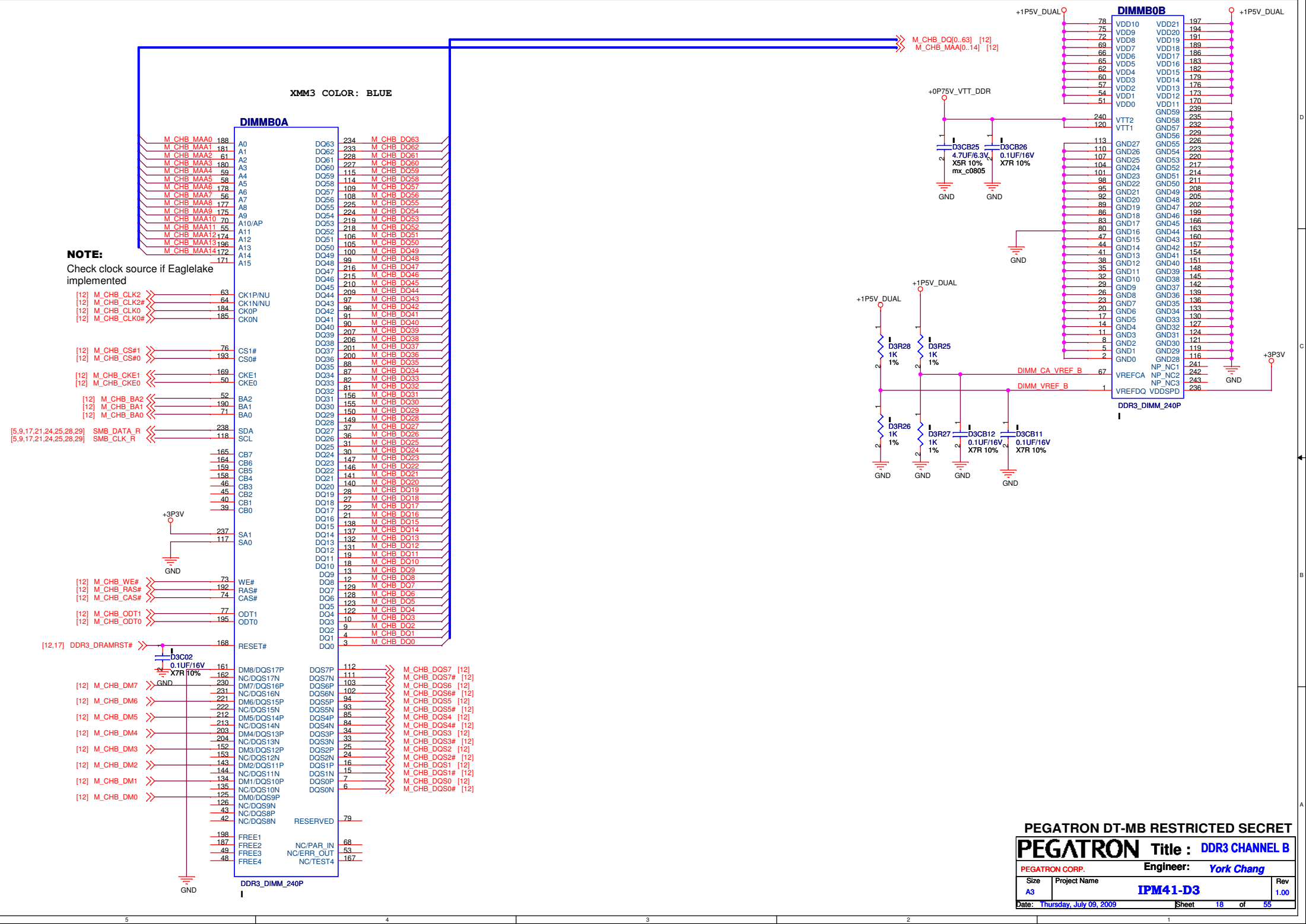
[12] M_CHA_WE# >> 73
[11] M_CHA_RAS# >> 192
[11] M_CHA_CAS# >> 74
[11] M_CHA_ODT1 >> 77
[11] M_CHA_ODT0 >> 195

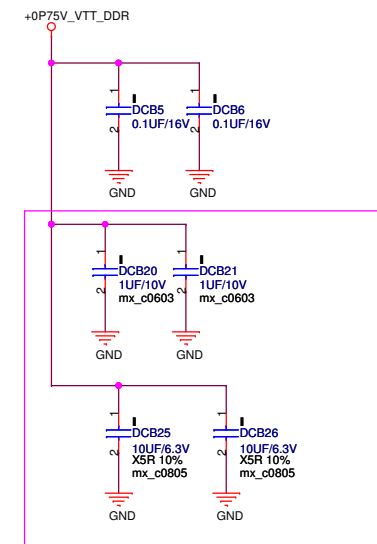
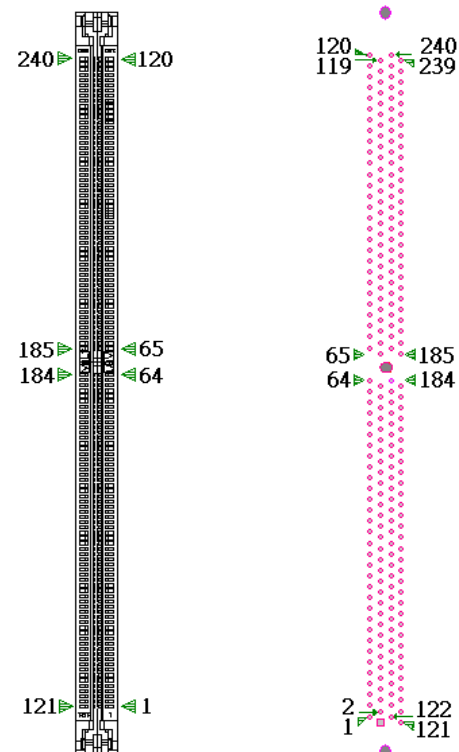
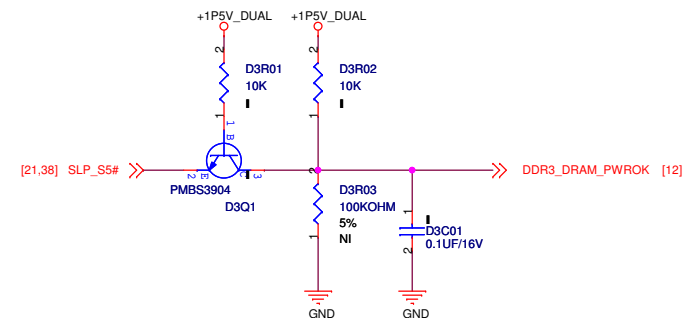
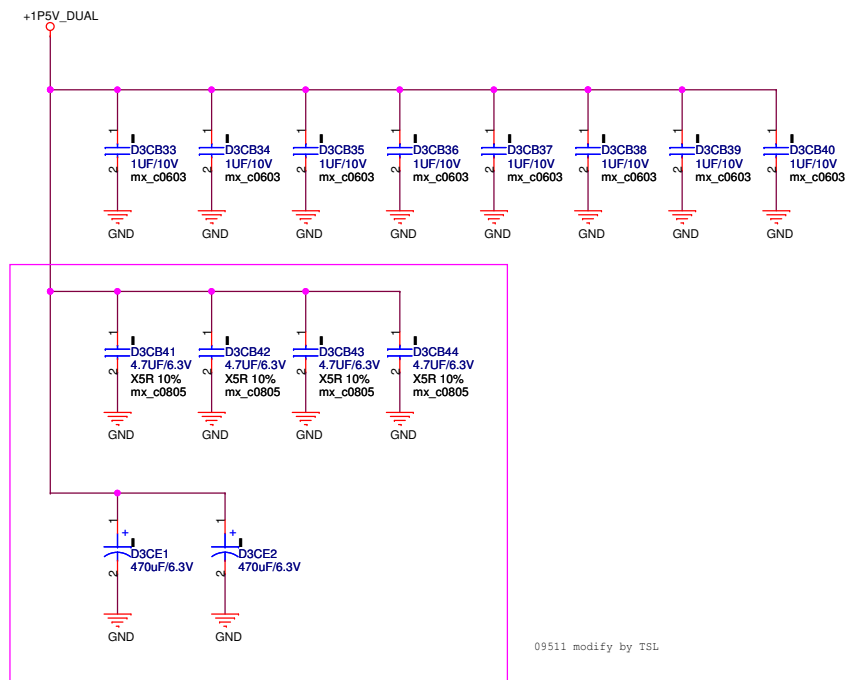
[12,18] DDR3_DRAMRST# >> 168
RESET#

[11] M_CHA_DM7 >> 161
[11] M_CHA_DM6 >> 230
[11] M_CHA_DM5 >> 231
[11] M_CHA_DM4 >> 221
[11] M_CHA_DM3 >> 222
[11] M_CHA_DM2 >> 212
[11] M_CHA_DM1 >> 213
[11] M_CHA_DM0 >> 203
[11] M_CHA_DM0 >> 204
[11] M_CHA_DM0 >> 152
[11] M_CHA_DM0 >> 153
[11] M_CHA_DM0 >> 143
[11] M_CHA_DM0 >> 144
[11] M_CHA_DM0 >> 134
[11] M_CHA_DM0 >> 135
[11] M_CHA_DM0 >> 125
[11] M_CHA_DM0 >> 126
[11] M_CHA_DM0 >> 43
[11] M_CHA_DM0 >> 42

FREE1 >> 198
FREE2 >> 187
FREE3 >> 49
FREE4 >> 48
NC/PAR_IN >> 68
NC/ERR_OUT >> 53
NC/TEST4 >> 167
RESERVED >> 79
DDR3_DIMM_240P



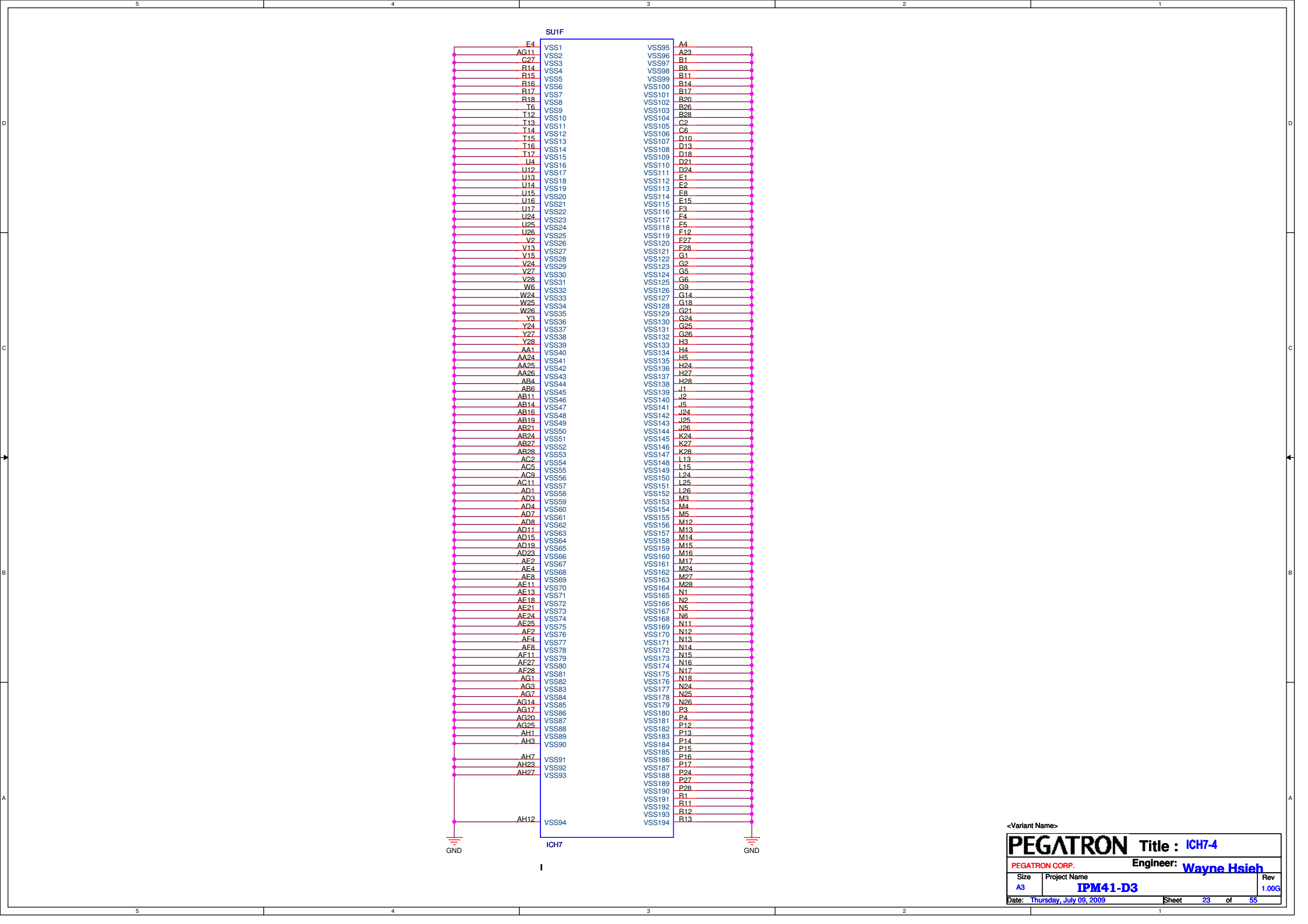




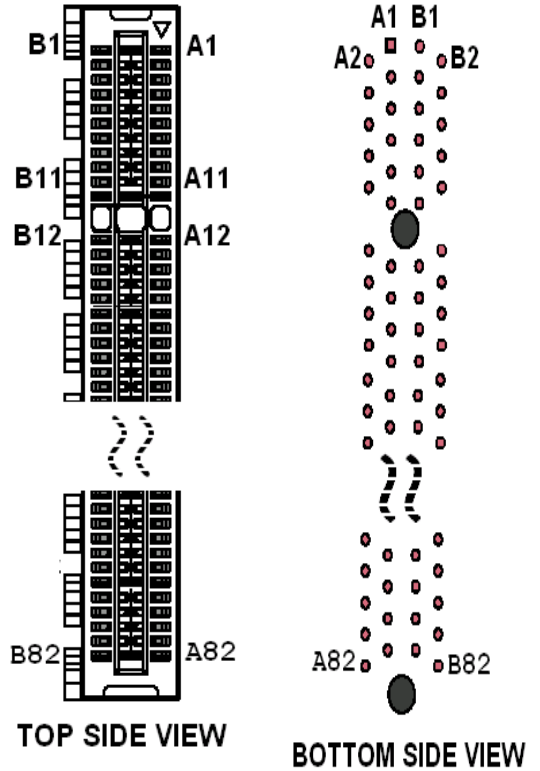
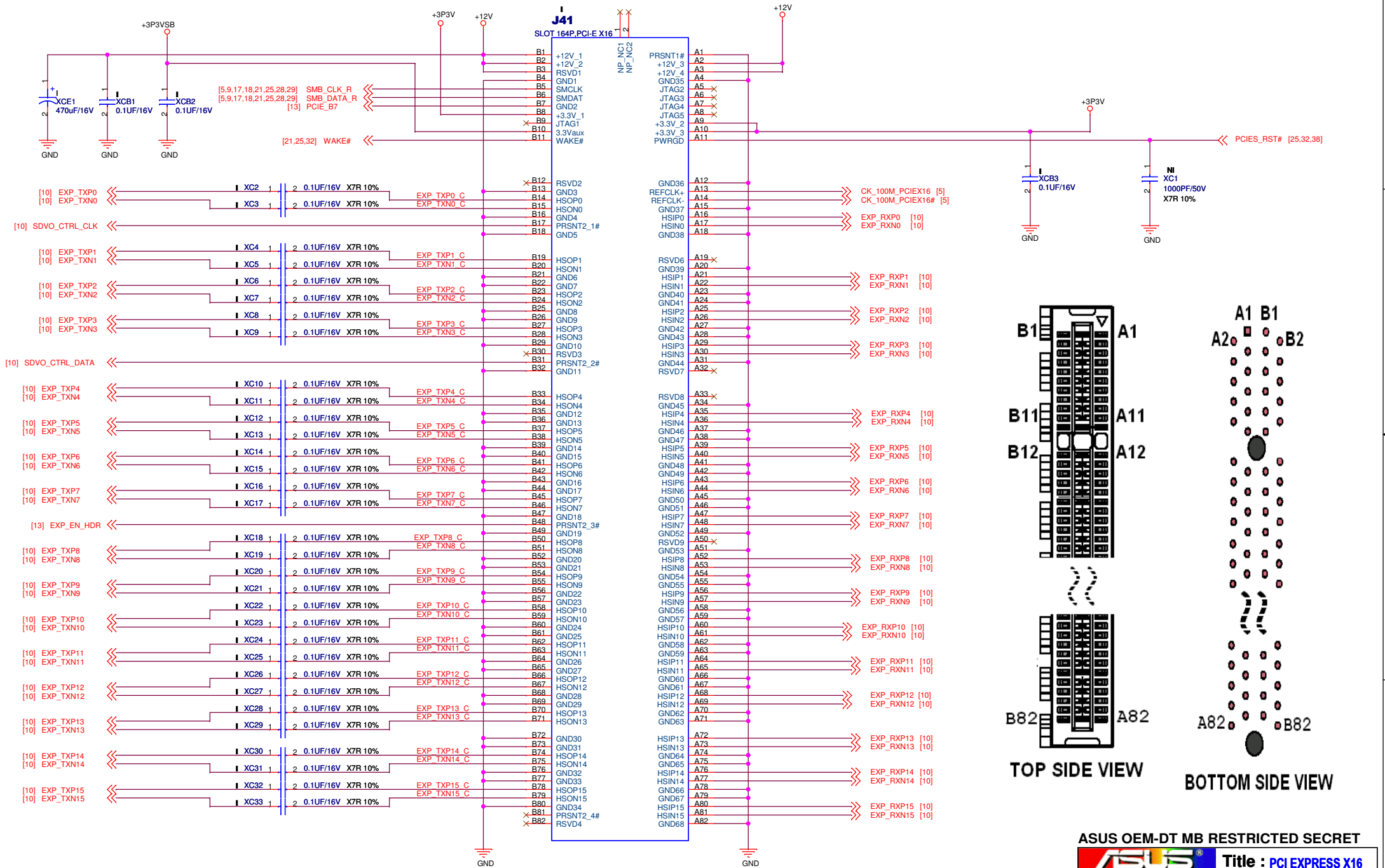
TOP SIDE VIEW EW BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

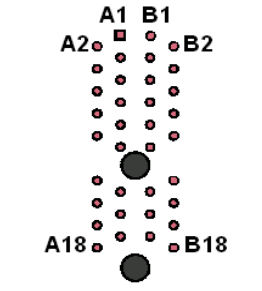
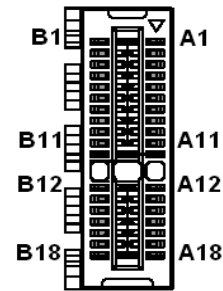
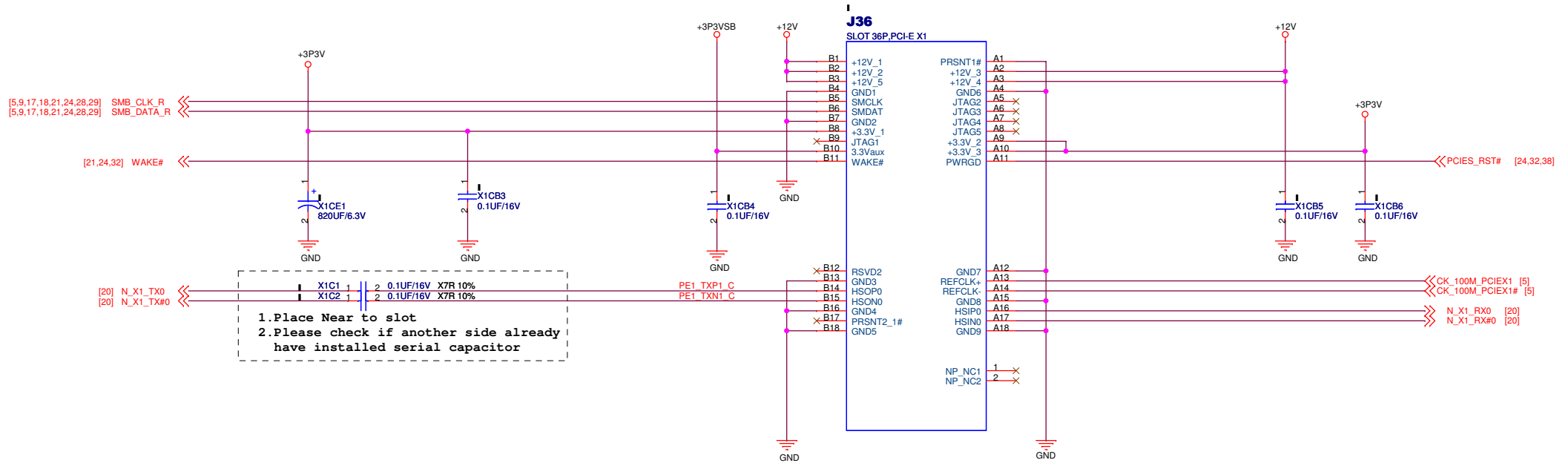
PEGATRON		Title : DECOUPLING	
PEGATRON CORP.		Engineer: York Chang	
Size A3	Project Name IPM41-D3	Rev 1.00	
Date: Thursday, July 09, 2009		Sheet 19 of 55	



PCI EXPRESS X16 Graphics Card Slot



PCI Express x1 SLOT



ASUS MBRD2_CET RESTRICTED SECRET

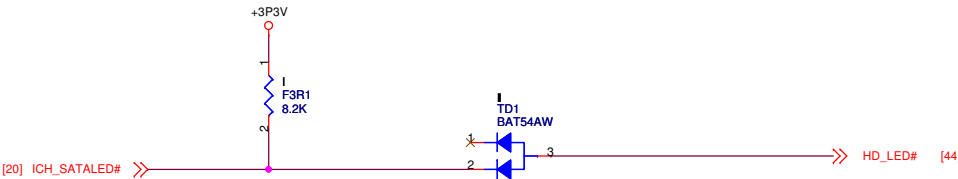
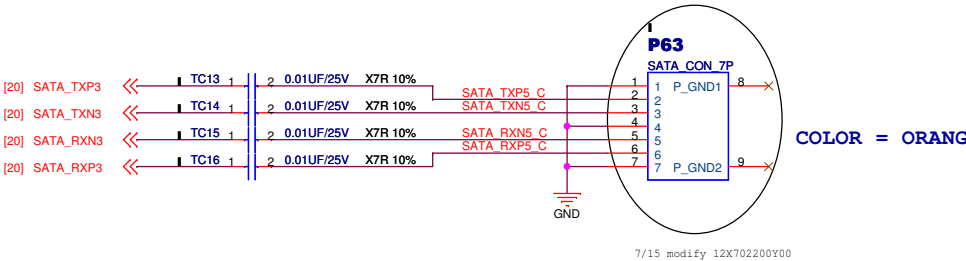
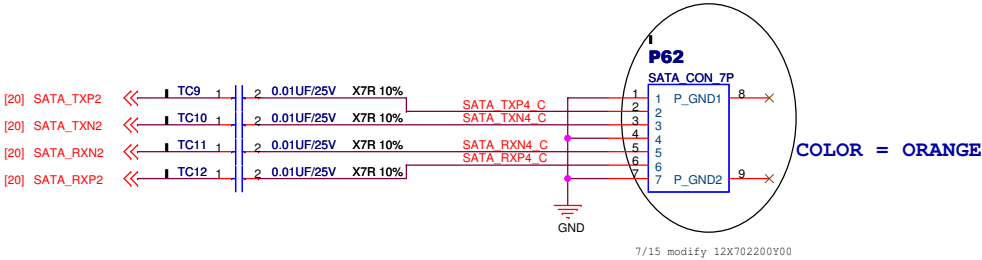
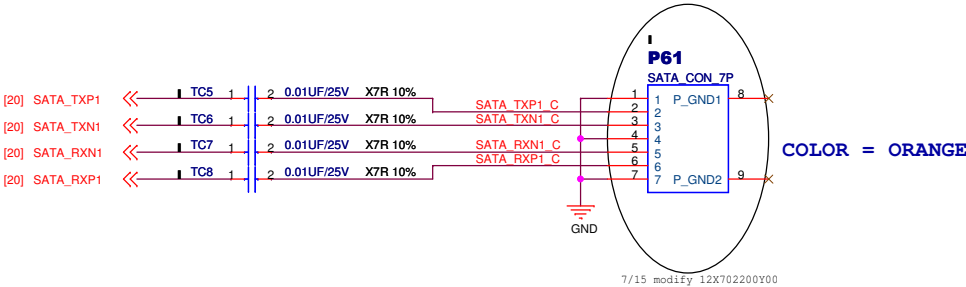
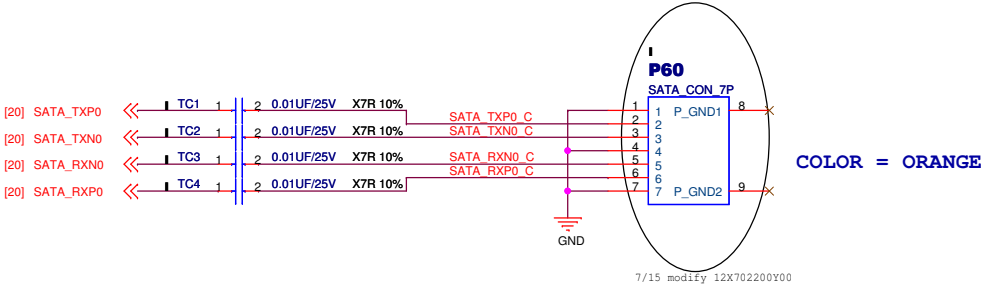
PEGATRON Title : **PCI EXPRESS X1**

PEGATRON CORP. Engineer: **Wayne Hsieh**

Size A3	Project Name IPM41-D3	Rev 1.00G
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Date: Thursday, July 09, 2009 Sheet 25 of 55

SATA CONNECTOR FOR BPC



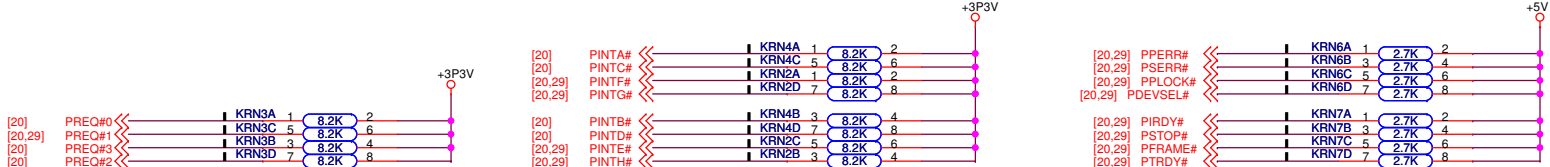
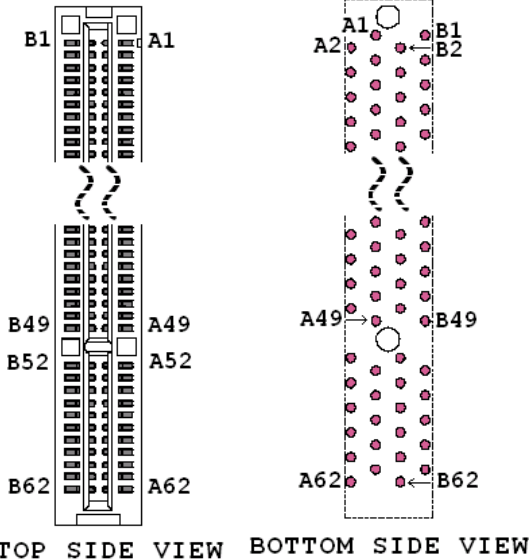
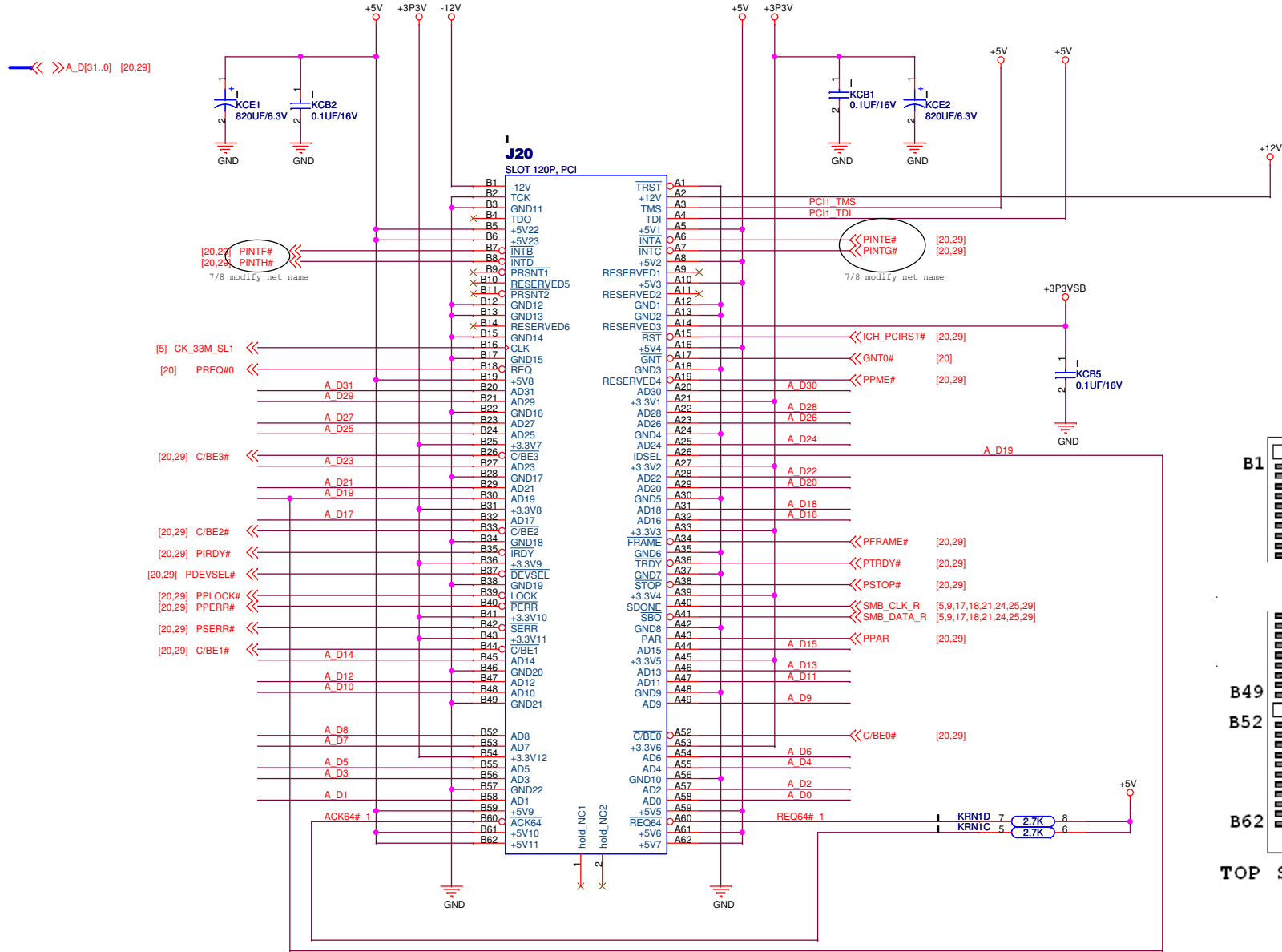
ASUS OEM-DT MB RESTRICTED SECRET

PEGATRON Title : SATA2 FOR BPC

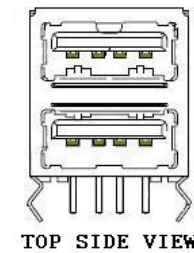
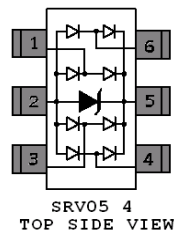
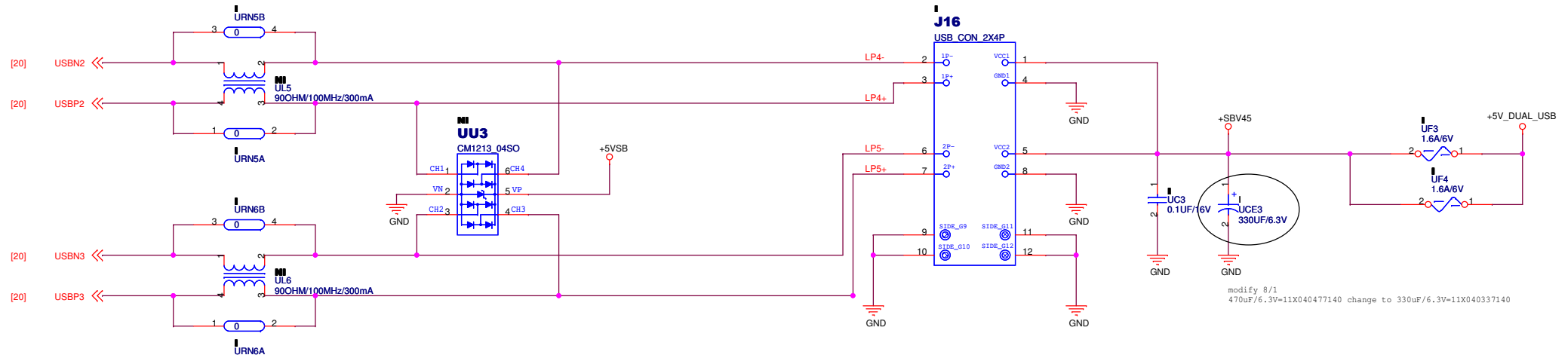
PEGATRON CORP. Engineer: Wayne Hsieh

Size A3 Project Name IPM41-D3 Rev 1.00G

Date: Thursday, July 09, 2009 Sheet 27 of 55



DOUBLE STACK PORT CONNECTOR FOR CPC



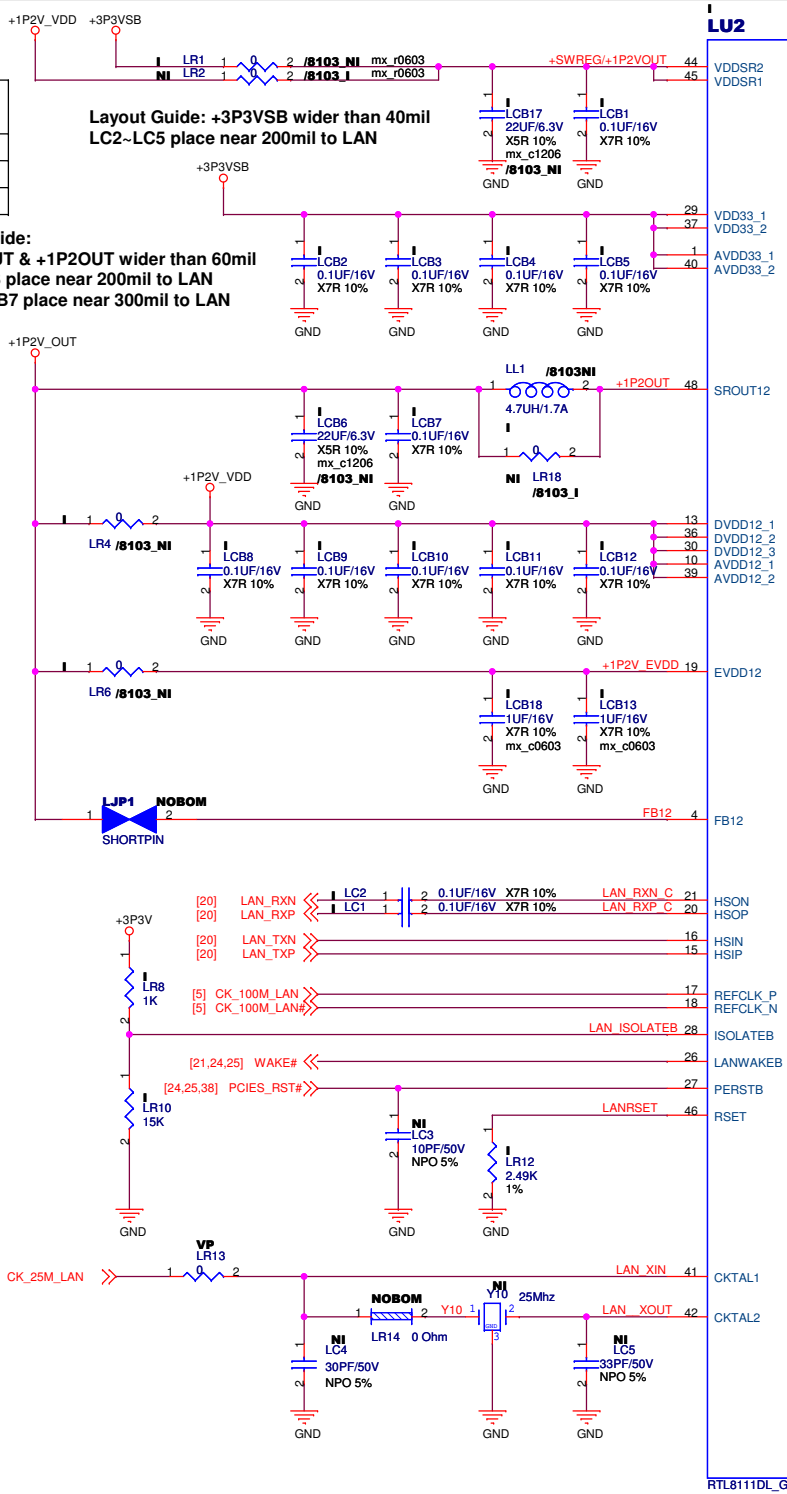
RTL8111DL Switching regulator

PIN	PIN NAME	I/O	Function
48	REG_OUT	O	Regulator output
4	FB12	I	Feedback pin
43	ENSWREG	I	3.3V : Enable ; 0V : disable
44,45	VDDREG	P	3.3V power pin

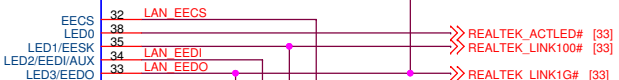
Layout Guide:
+1P2V_OUT & +1P2OUT wider than 60mil
LL1&LR18 place near 200mil to LAN
LCB6&LCB7 place near 300mil to LAN

8103EL	Pin
DVDD3.3V	29,37
AVDD3.3V	1
DVDD1.2V	10,13,30,36
+1.2V_OUT	19,45,48

8111DL	Pin
DVDD3.3V	29,37
AVDD3.3V	1,40
DVDD1.2V	13,36
AVDD1.2V	10,30,39
EVDD1.2V	19
+1.0V_OUT	48



LU2

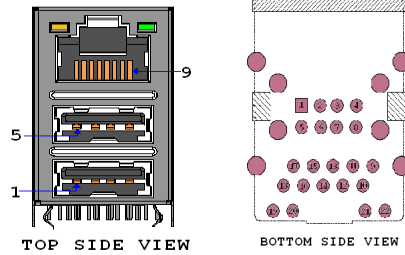
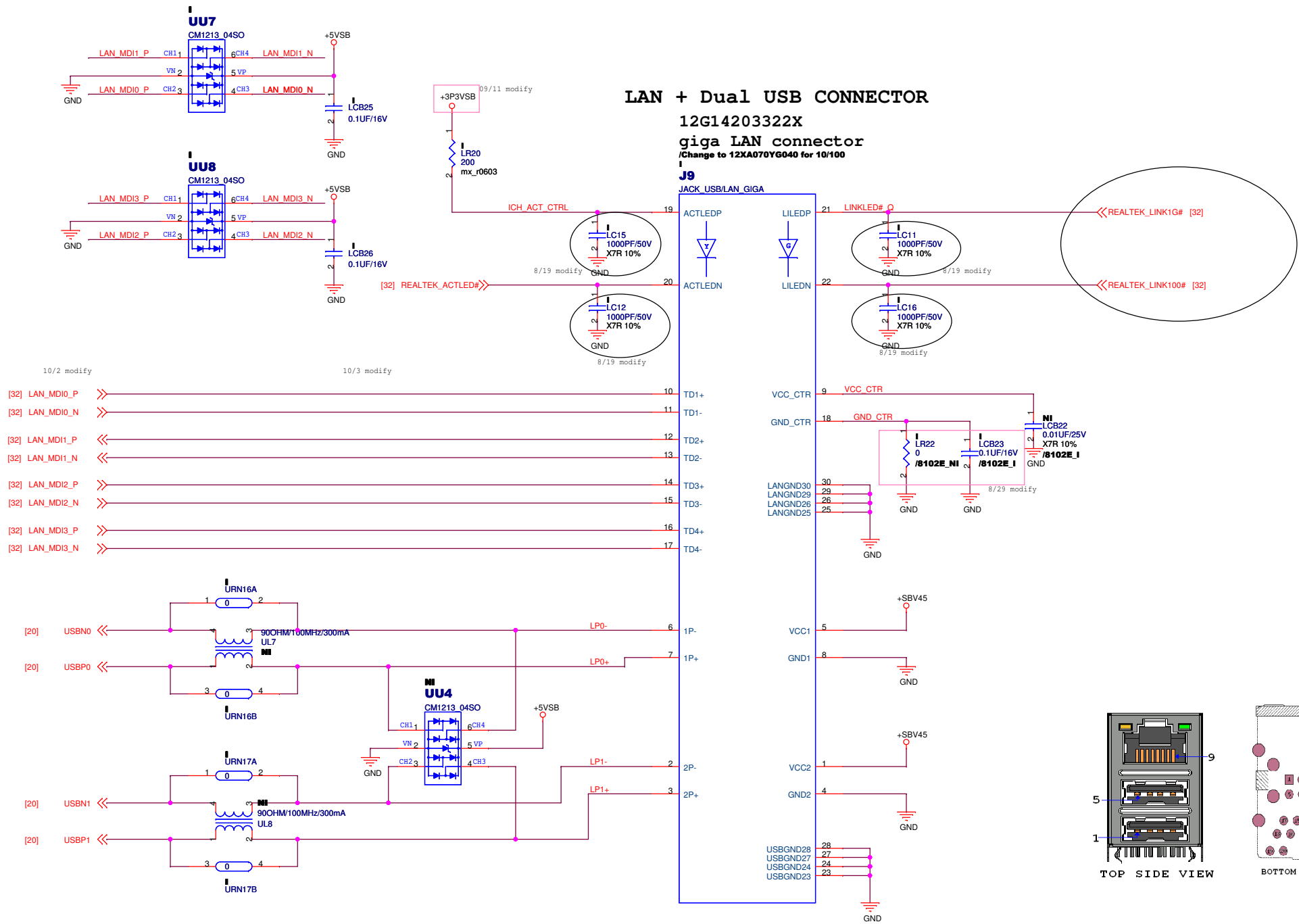


NOTE:
If using eFuse function,
NI LU2 directly

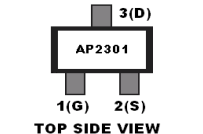
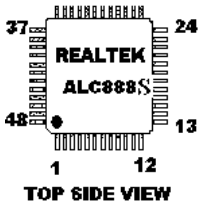
NOTE: LED MODE
(LEDS1, LEDSO) = (1, 1) DEFAULT
(LEDS1, LEDSO) = (0, 1) ==> For this schematic

NOTE: 8111DL[PIN43]
3.3V enable internal regulator
0V disable internal regulator

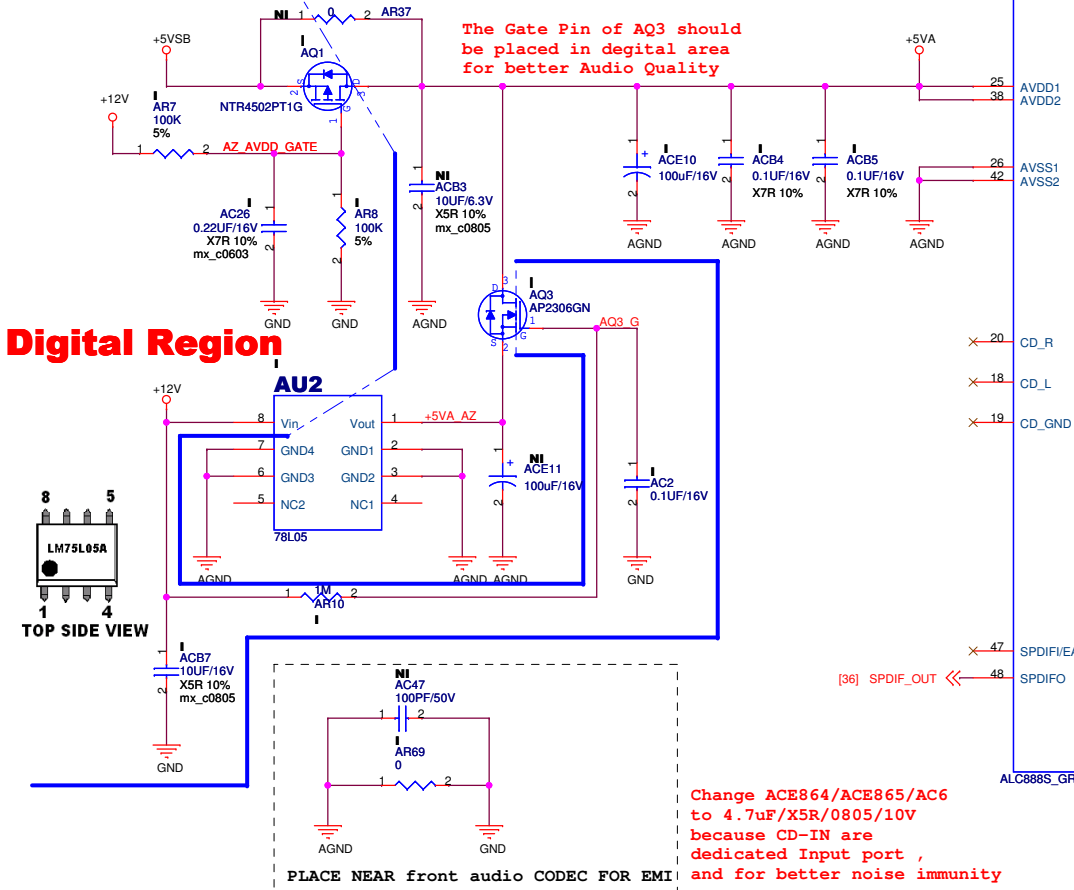
Symbol	Type	Pin No (64-pin)	Pin No (48-pin)	Description
LED0	O	57	38	LEDS1-0
LED1	O	56	35	LED0 Tx/Rx
LED2	O	55	34	LED1 Tx/Rx
LED3	O	54	33	LED2 Tx/Rx



	ALC888S-B1	ALC888S-VC2
Pin 4	DVSS	GPIO1/DMIC-DATA



Please noite:
AZ_BITCLK need add
a serial res(22 ohm)
near SB side



Digital Region

Provision AR23 for
ALC888S-VC2 codec

The Gate Pin of AQ3 should
be placed in digital area
for better Audio Quality

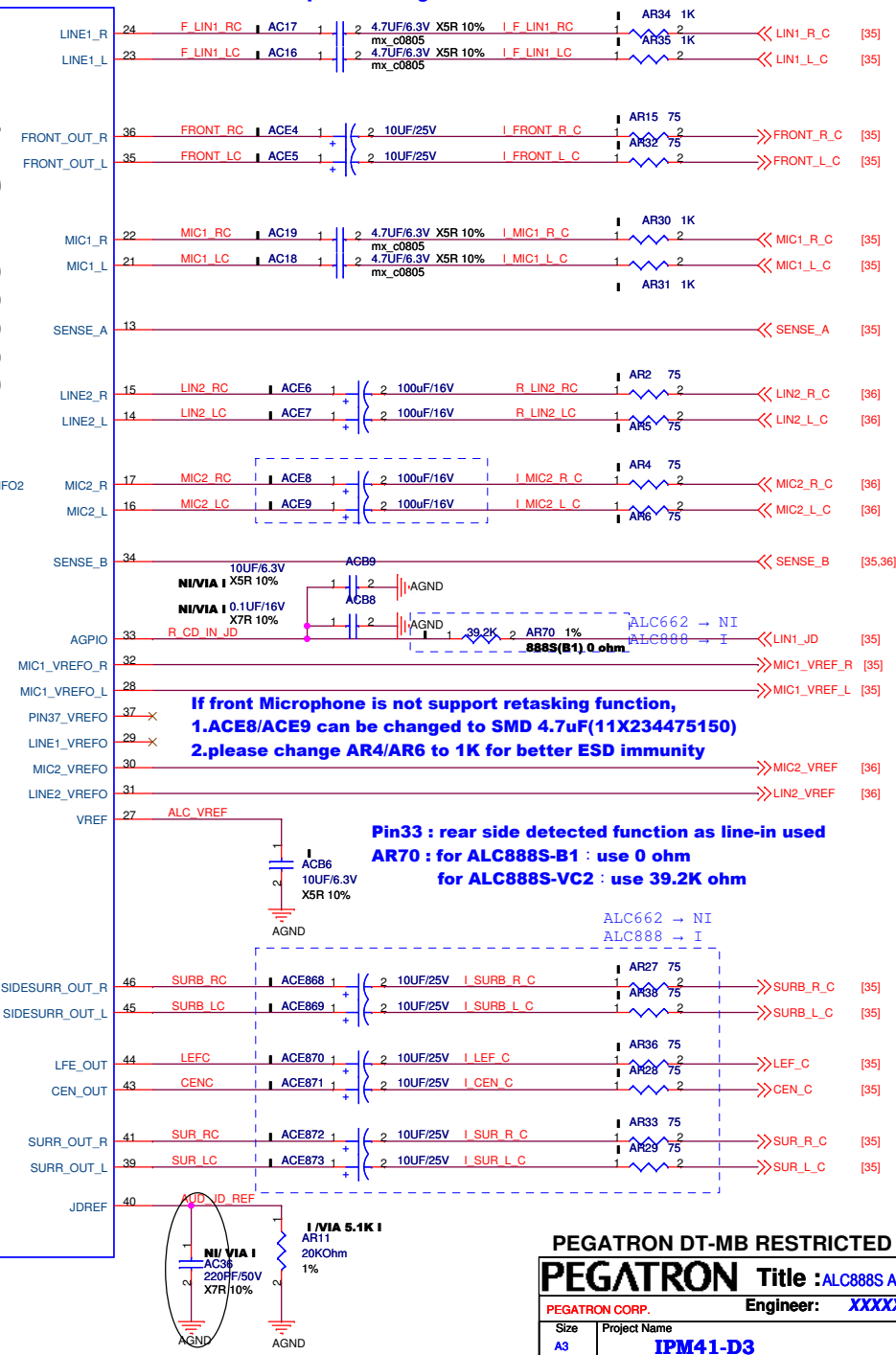
PLACE NEAR front audio CODEC FOR EMI

Change ACE864/ACE865/AC6
to 4.7uF/X5R/0805/10V
because CD-IN are
dedicated Input port ,
and for better noise immunity

C.S ALC662-GR LQFP-48 : 02G611003200
C.S ALC888S-GR(B1) LQFP-48 : 02G611003510
C.S ALC888S-VC2-GR LQFP-48 : 02G611003521

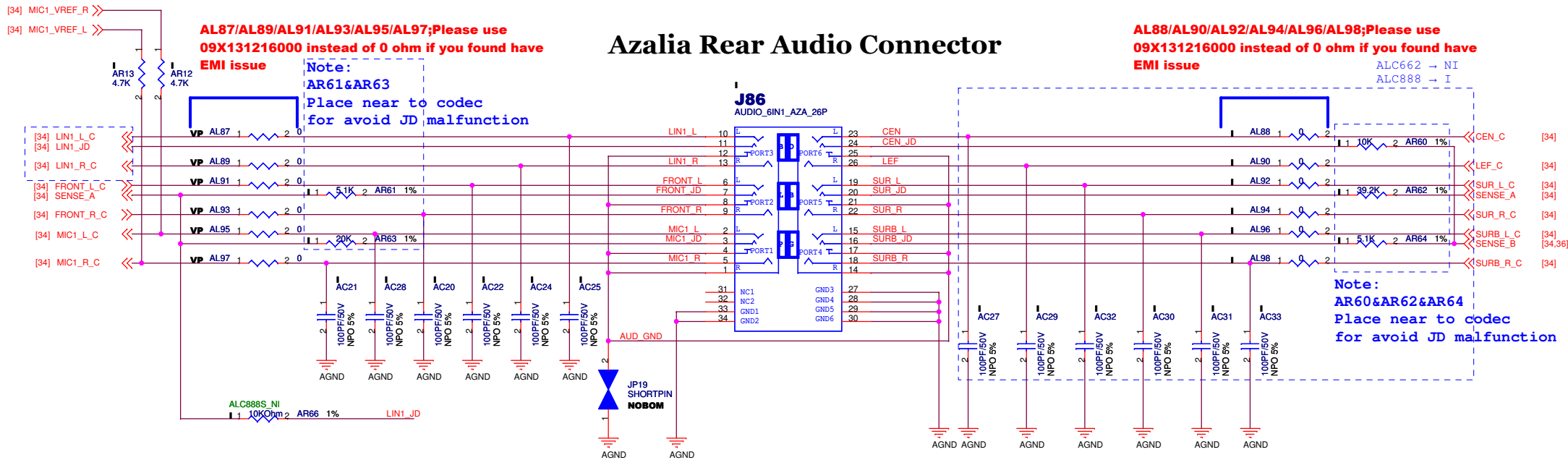
ALC888S Rev. A

If pin 23/24 and pin 21/22 support retasking function,
please changed AR34/AR35/AR30/AR31 to 75 ohm



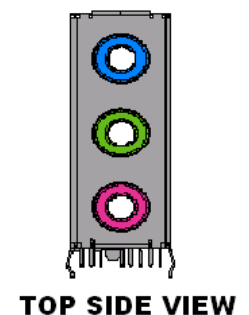
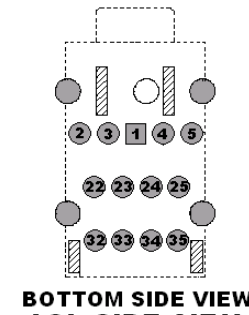
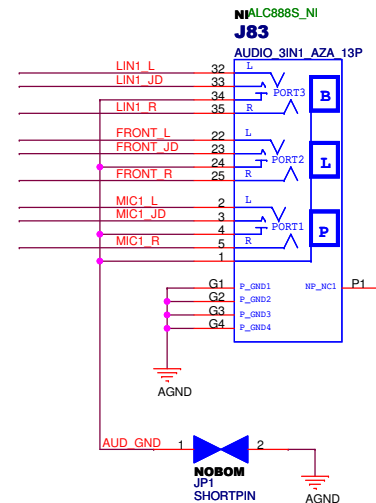
If front Microphone is not support retasking function,
1.ACE8/ACE9 can be changed to SMD 4.7uF(11X234475150)
2.please change AR4/AR6 to 1K for better ESD immunity

Pin33 : rear side detected function as line-in used
AR70 : for ALC888S-B1 : use 0 ohm
for ALC888S-VC2 : use 39.2K ohm



Azalia Rear Audio Connector

Note:
Rear Side Audio Header Just Only Function Dedicated



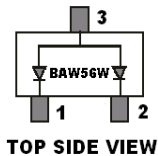
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : HP AUDIO CONNECTOR

PEGATRON CORP. Engineer: XXXXX_XX

Size A3 Project Name IPM41-D3 Rev 1.00

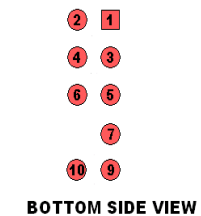
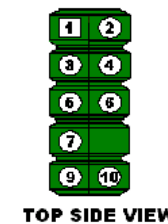
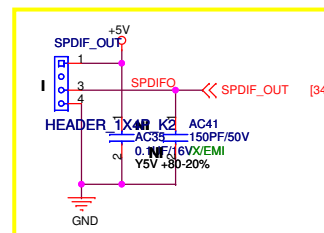
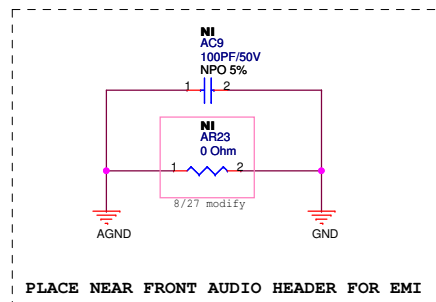
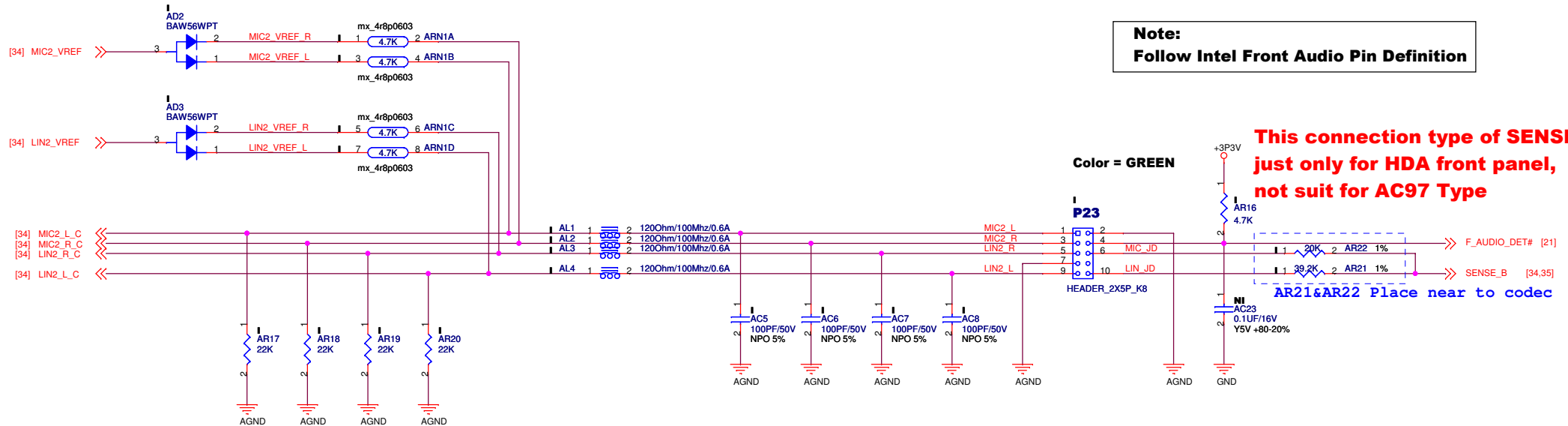
Date: Thursday, July 09, 2009 Sheet 35 of 55

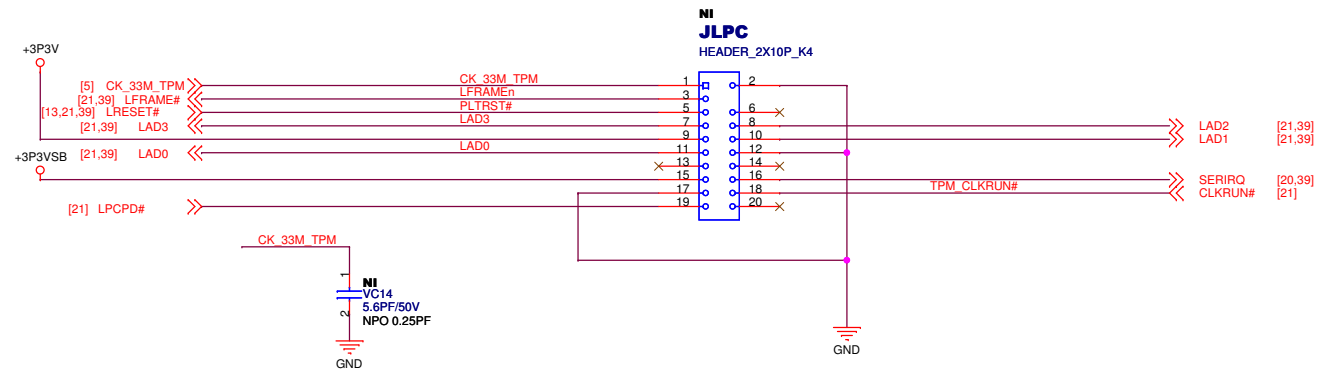


Note:
Front Side Support MIC&Headphone&Re-tasking Function

Azalia Front Audio Header

Note:
Follow Intel Front Audio Pin Definition





TOP SIDE VIEW



BOTTOM SIDE VIEW

ASUS OEM-DT MB RESTRICTED SECRET

PEGATRON Title : **TPM HEADER**

PEGATRON CORP. Engineer: **Wayne Hsieh**

Size Project Name **IPM41-D3** Rev 1.00G

Date: Thursday, July 09, 2009 Sheet 37 of 55

TOP SIDE VIEW

BOTTOM SIDE VIEW

TOP SIDE VIEW

PORT ADDRESS TRAPING -> HEFRAS

: During power on reset, it is internal PD

RTS1#	CONFIG PORT ADDR
0	0x002E
1	0x004E

ROM TRAPING -> DTR1#

: During power on reset, it is internal PD

DTR1#	PENROM
0	DISABLE
1	ENABLE

KEYBOARD TRAPING -> PENKBC

: During power on reset, it is internal PD

TXD1	KEYBOARD
0	DISABLE
1	ENABLE

83627DHG(C) 02X230362760

02G230362761
C.S W83627DHG-A(C) PQFP128 WINBOND (SORT)

ASUS OEM-DT MB RESTRICTED SECRET

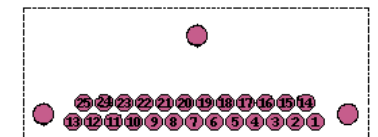
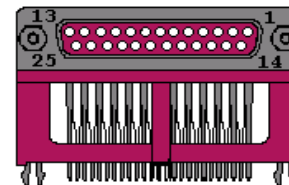
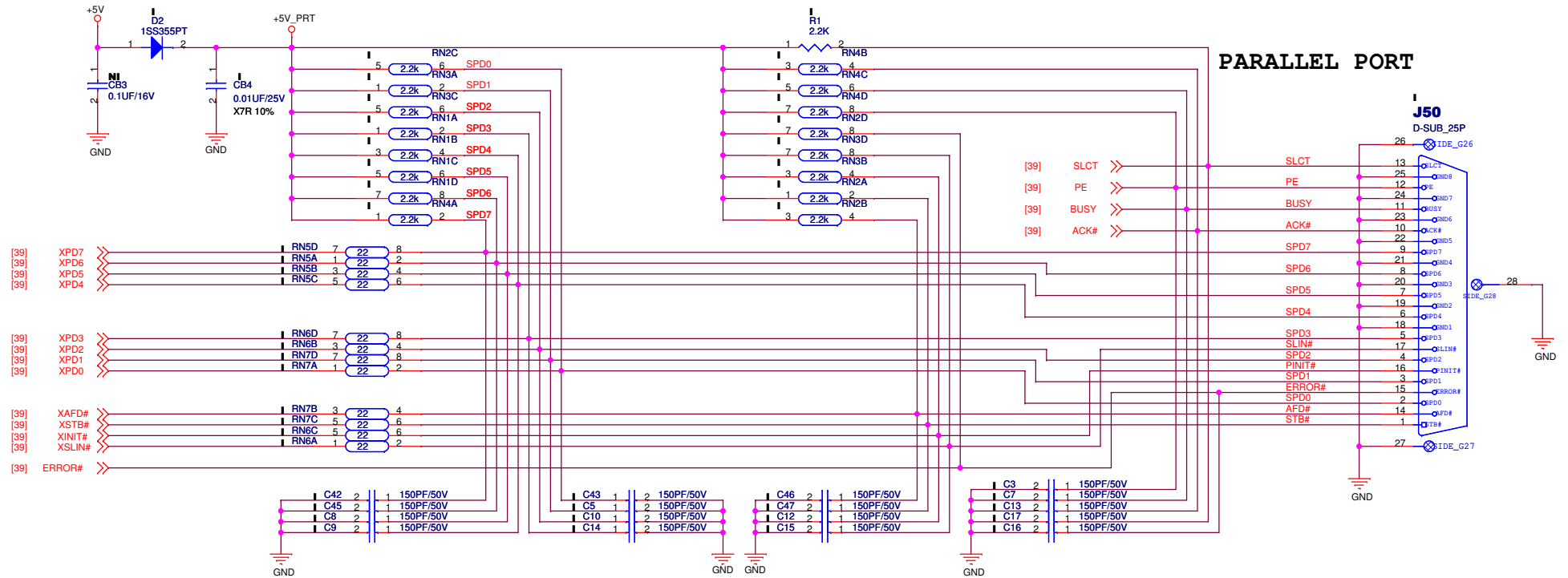
PEGATRON Title : SIO W83627DHG 2-2

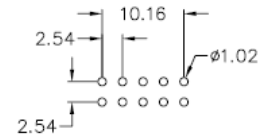
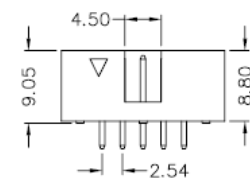
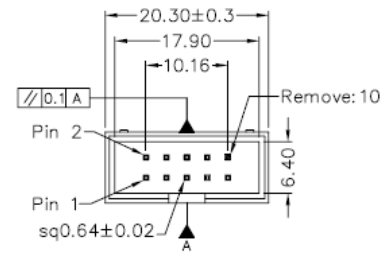
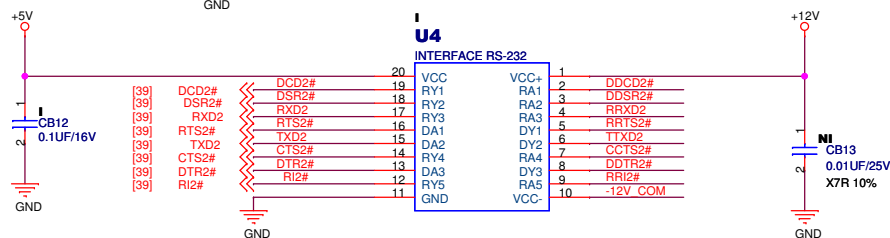
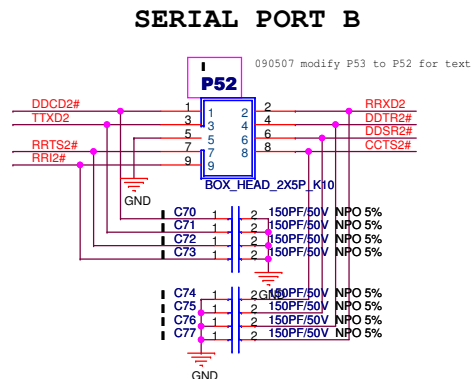
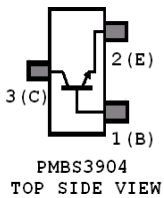
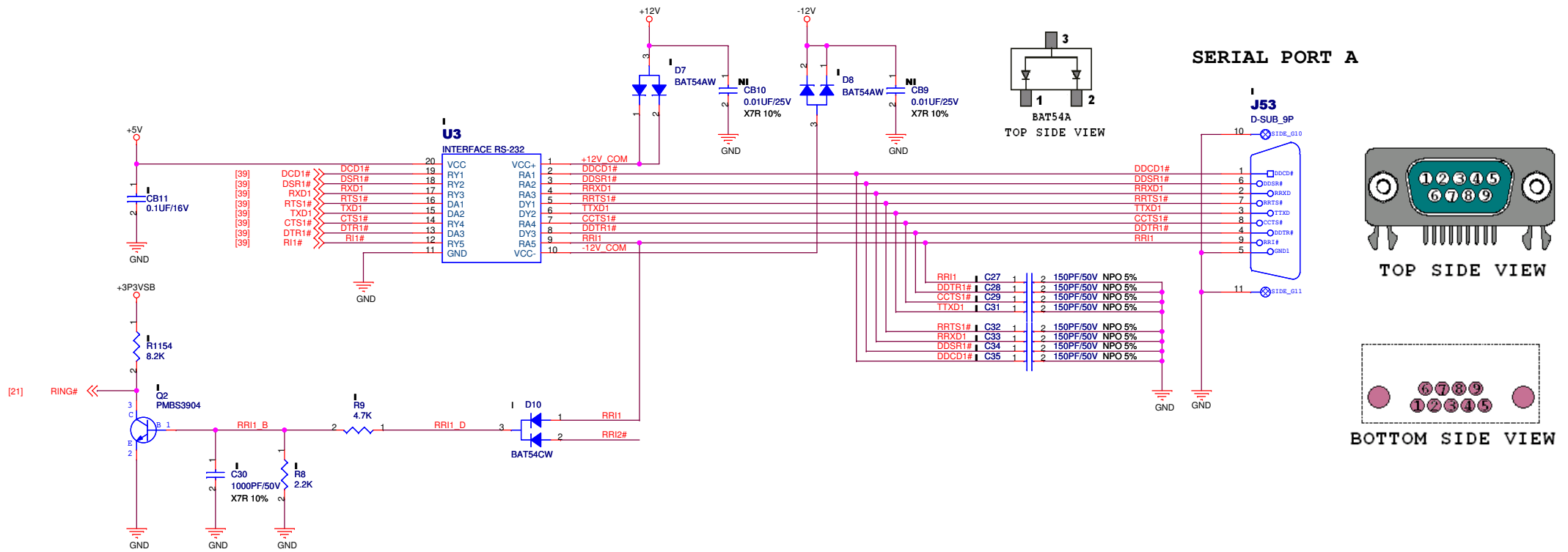
PEGATRON CORP. Engineer: Wayne Hsieh

Size A3 Project Name IPM41-D3 Rev 1.00G

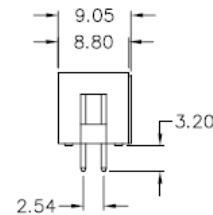
Date: Thursday, July 09, 2009 Sheet 39 of 55

<< FOR CPC >>

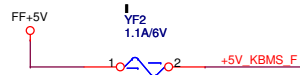




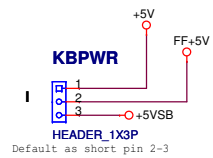
Recommended P.C.B Layout



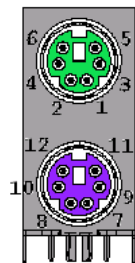
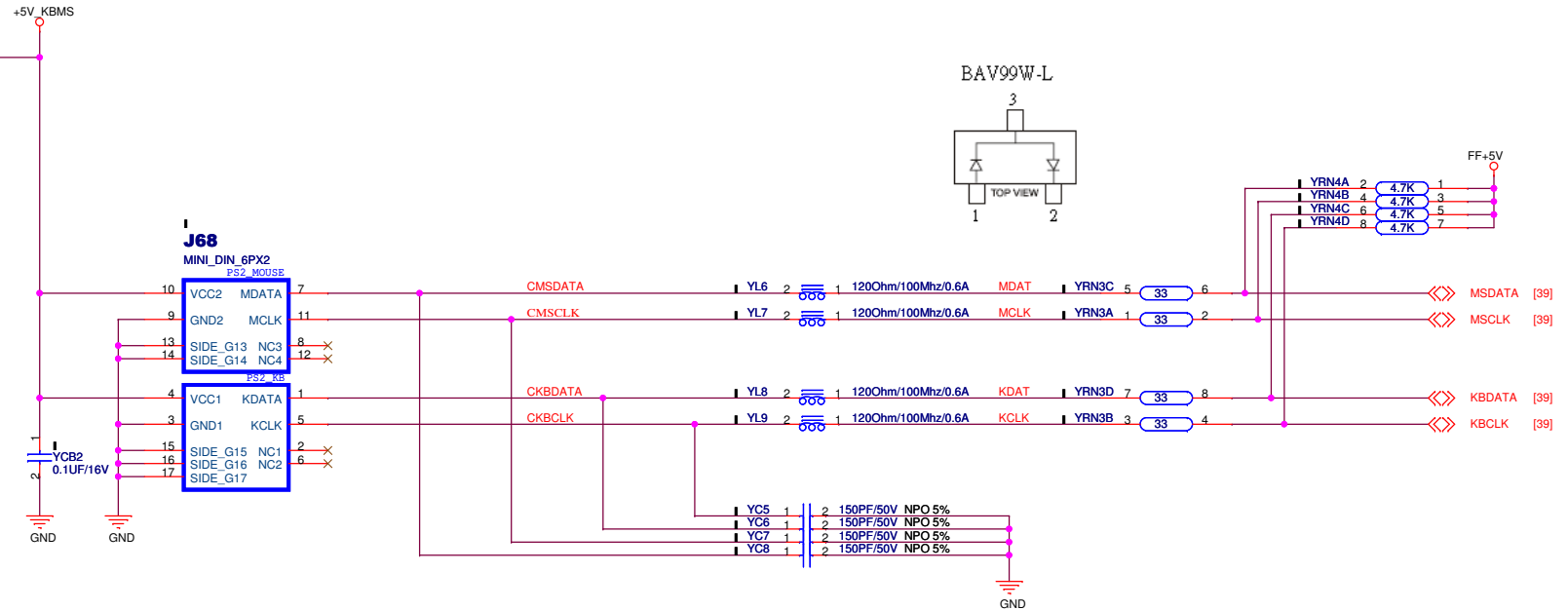
PS/2 KEYBOARD & MOUSE FOR CPC



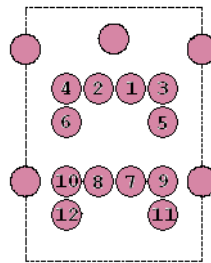
Note:
The +5V_DUAL_USB_B power trace width must have 40 mils or more



KBPWR:
1-2: +5V
2-3: +5VSB
KBPWR:23
MINI_JUMPER



TOP SIDE VIEW



BOTTOM SIDE VIEW

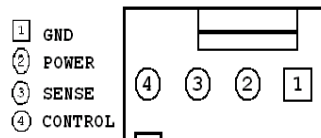
ASUS MBRD2_CEC RESTRICTED SECRET

PEGATRON Title : KB & MS FOR CPC

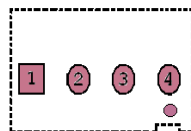
PEGATRON CORP. Engineer: Wayne Hsieh

Size A3 Project Name IPM41-D3 Rev 1.006

Date: Thursday, July 09, 2009 Sheet 42 of 55



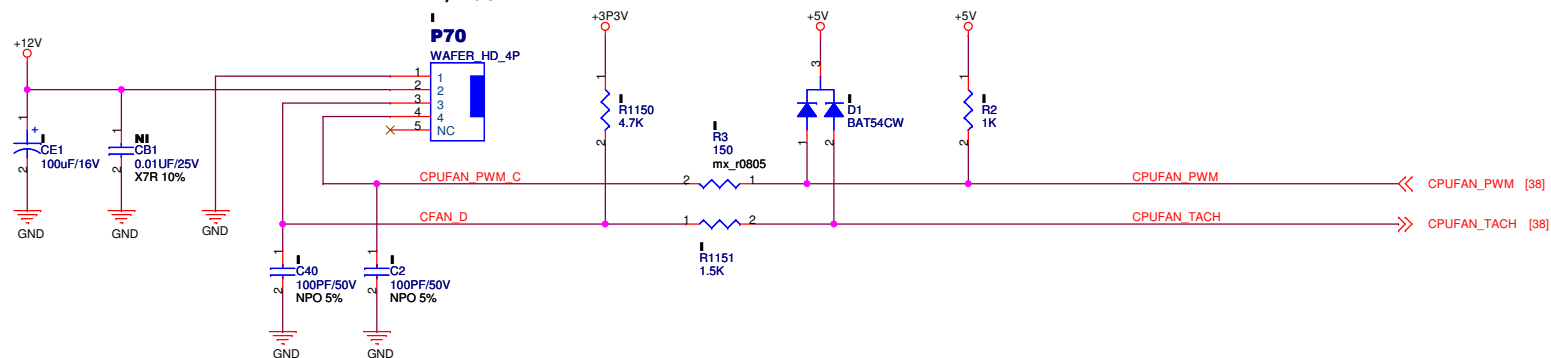
TOP SIDE VIEW



BOTTOM SIDE VIEW

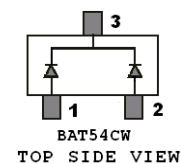
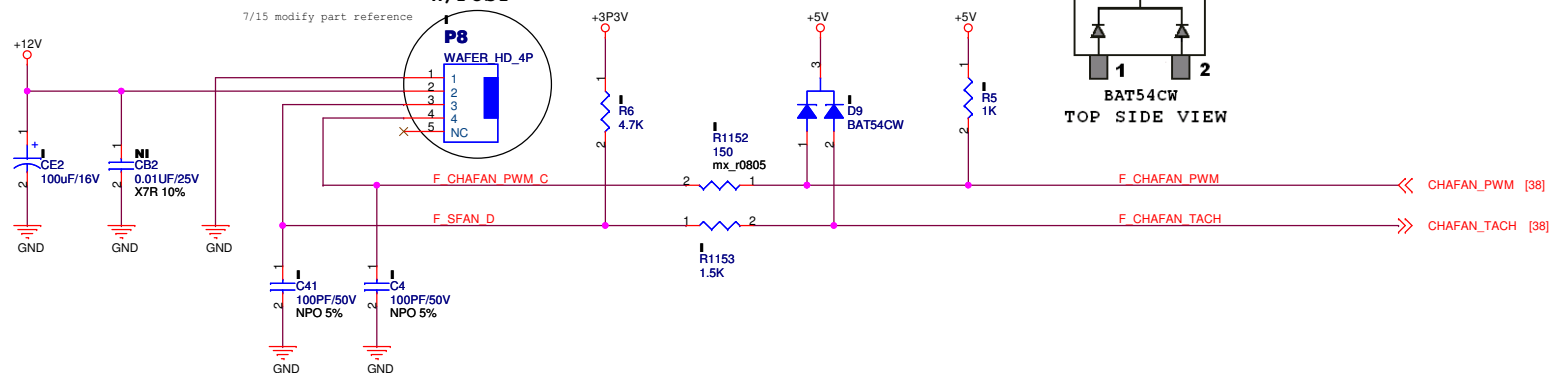
CPU FAN COLOR: WHITE W/POST

P70
WAFER_HD_4P



CHASIS FAN COLOR: WHITE W/POST

P8
WAFER_HD_4P



ASUS OEM-DT MB RESTRICTED SECRET

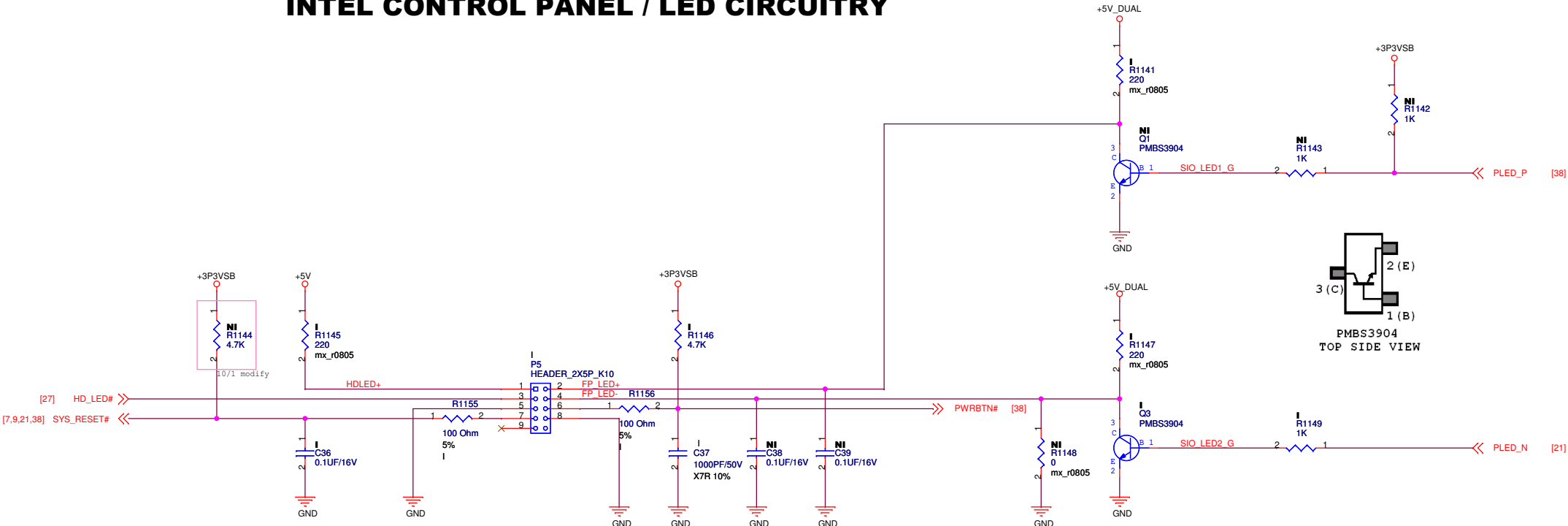
PEGATRON Title : 4-PIN FAN CONN

PEGATRON CORP. Engineer: Wayne Hsieh

Size A3 Project Name IPM41-D3 Rev 1.006

Date: Thursday, July 09, 2009 Sheet 43 of 55

INTEL CONTROL PANEL / LED CIRCUITRY

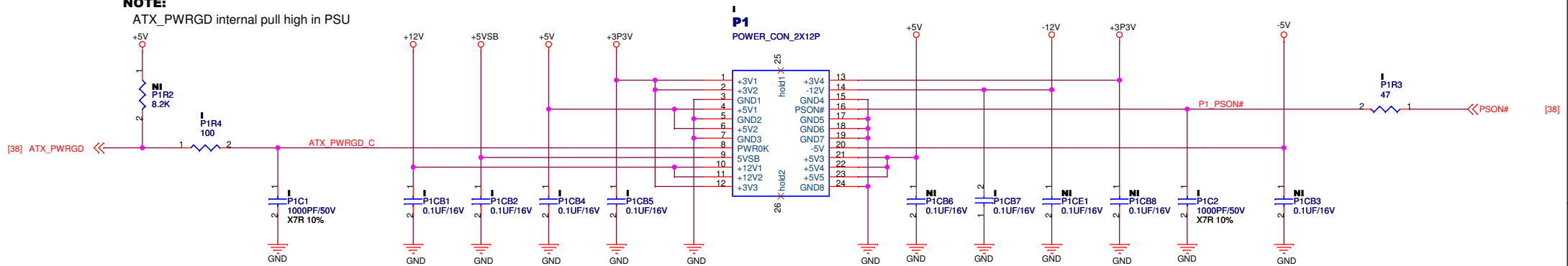


FRONT POWER LED COLOR SUPPORT	R10	Q2	R6	R11
SINGLE COLOR	I	NI	NI	NI
DUAL COLOR	NI	I	I	I

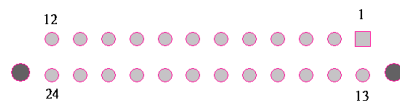
ATX POWER_24P SUPPLY CONNECTOR

NOTE:

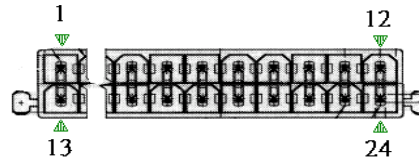
ATX_PWRGD internal pull high in PSU



All of the Caps Around the ATX Power Connector

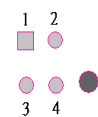
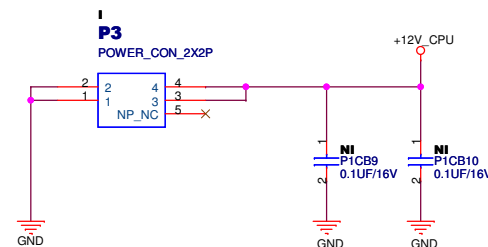


BOTTOM SIDE VIEW

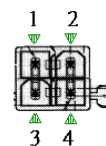


TOP SIDE VIEW

VRM POWER_4P SUPPLY CONNECTOR



BOTTOM SIDE VIEW



TOP SIDE VIEW

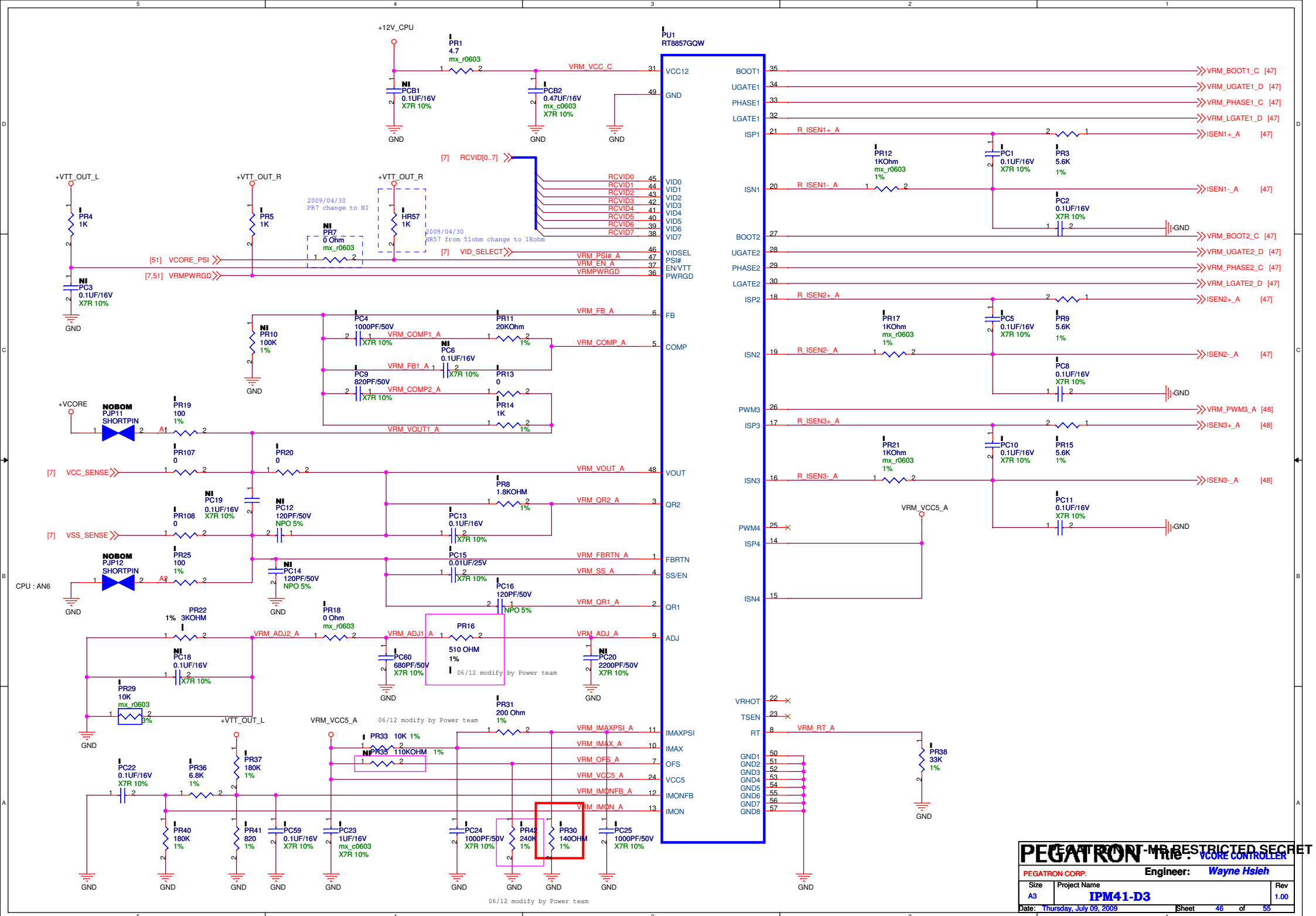
ASUS OEM-DT MB RESTRICTED SECRET

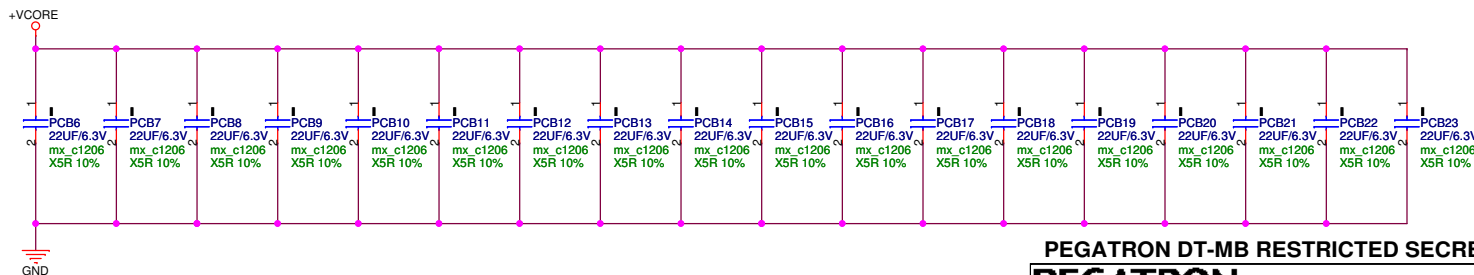
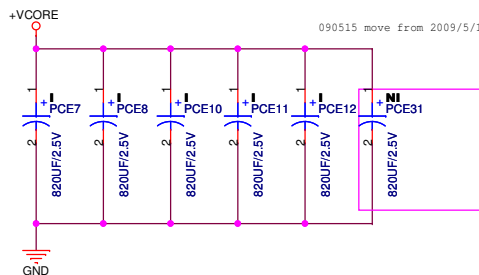
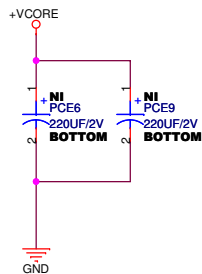
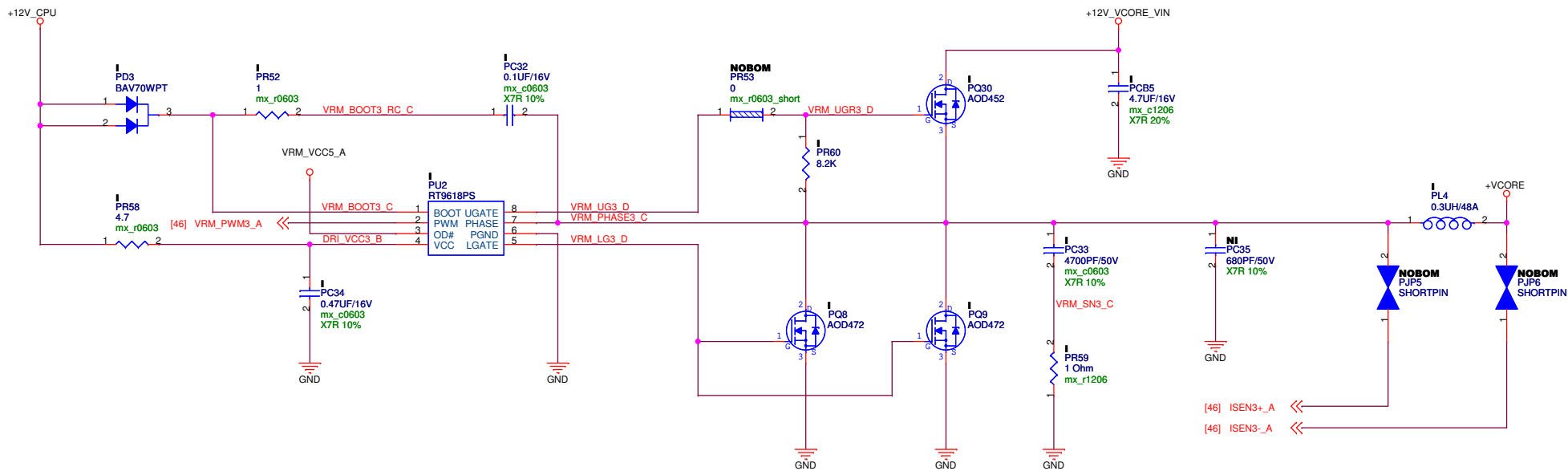
PEGATRON Title : **ATX POWER**

PEGATRON CORP. Engineer: **Wayne Hsieh**

Size A3 Project Name **IPM41-D3** Rev 1.00G

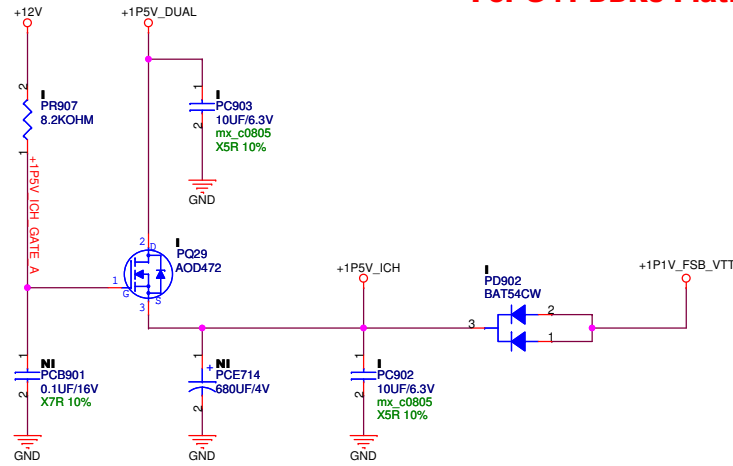
Date: Thursday, July 09, 2009 Sheet 45 of 55



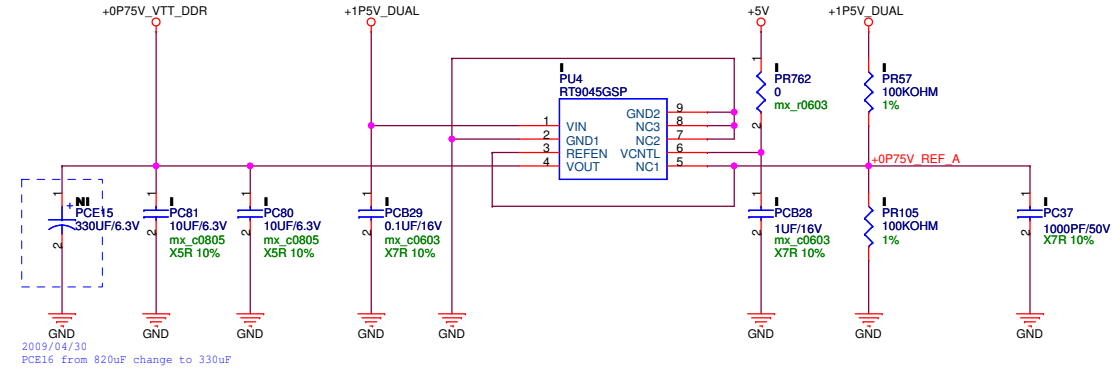


+CPU Vcore OUTPUT CAPs

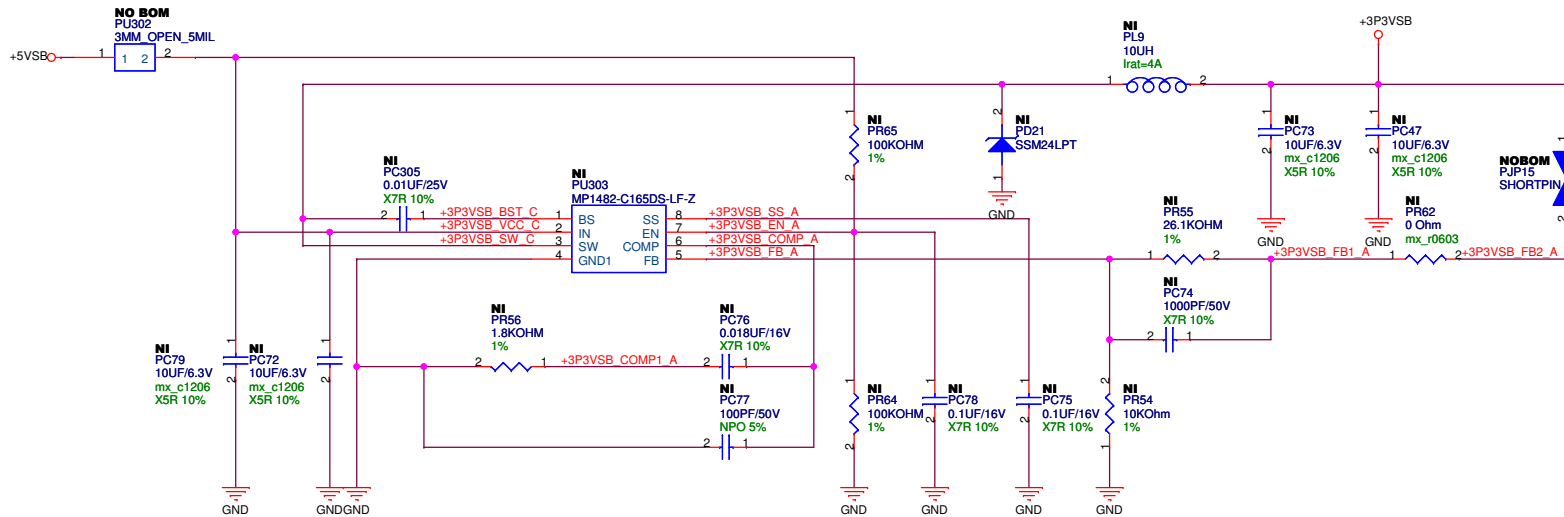
+1P5V_ICH (2A) **For G41 DDR3 Platform**



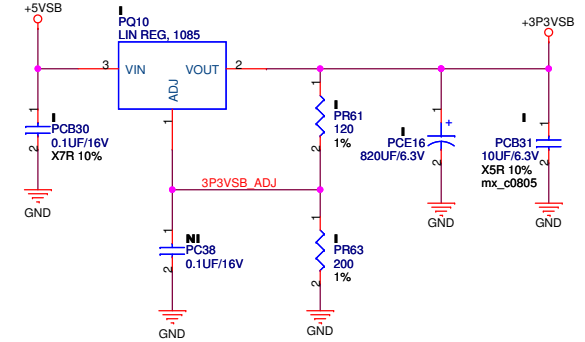
+1P5V_DUAL → +0P75V_VTT_DDR (1A)



+5VSB → +3P3VSB (1.5A) **Eup 1W**

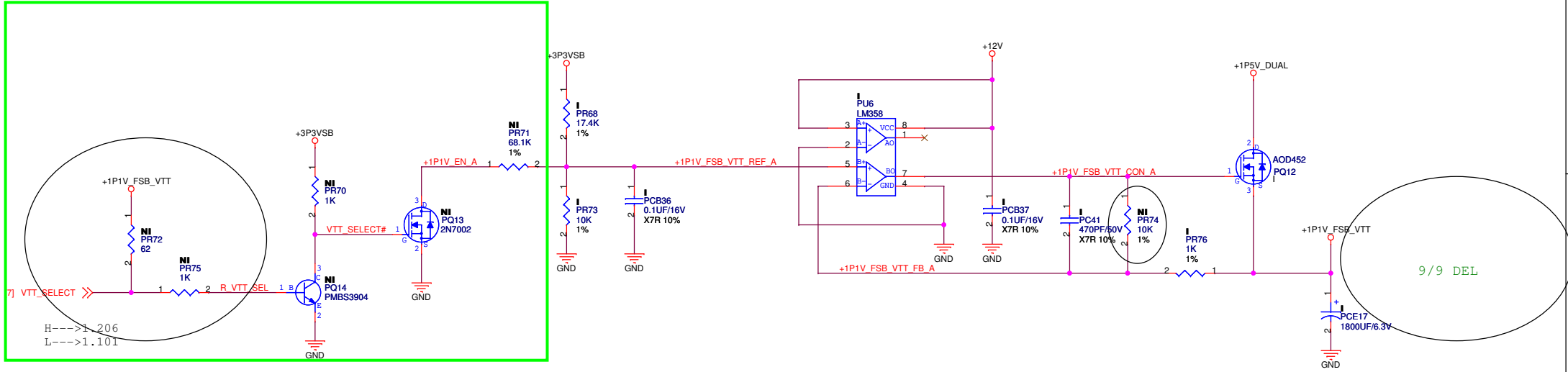


+5VSB ==> +3P3VSB (1.5A)



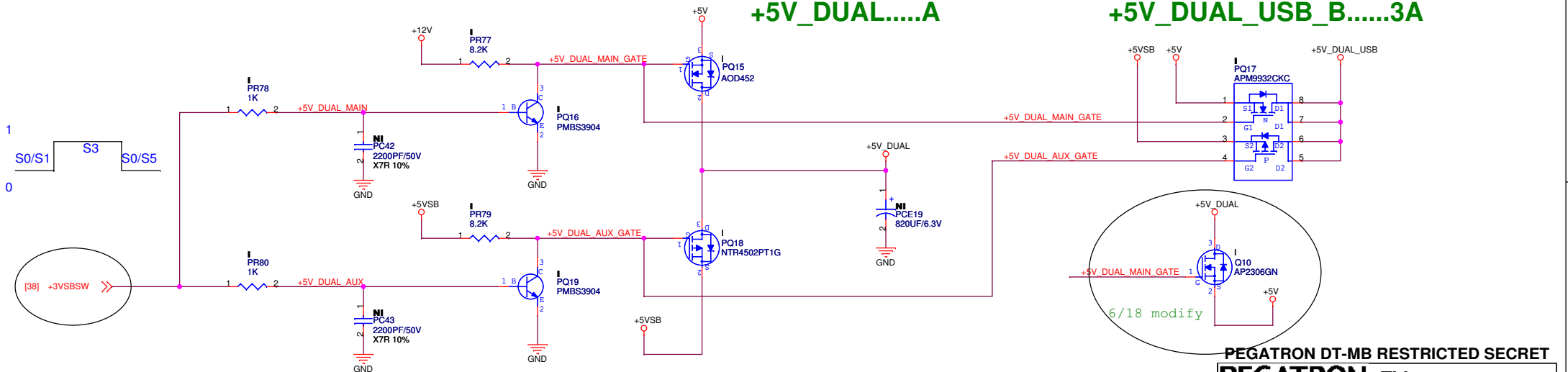
+1P5V_DUAL ==> +1P1V_FSB_VTT (1.5A) **Fixed in 1.2V**

change to NI in 9/9

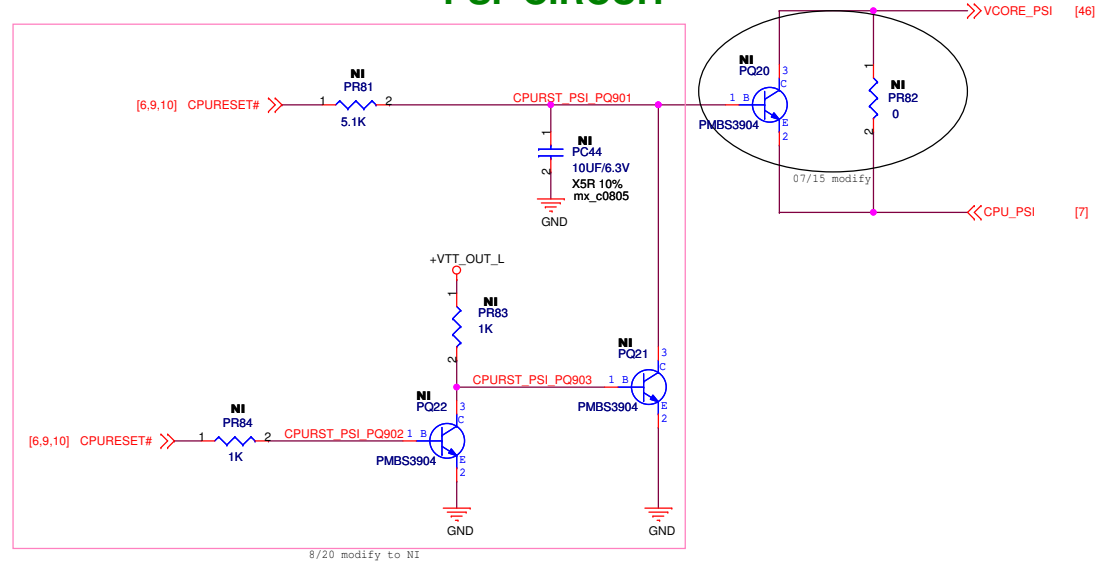


+5V_DUAL.....A

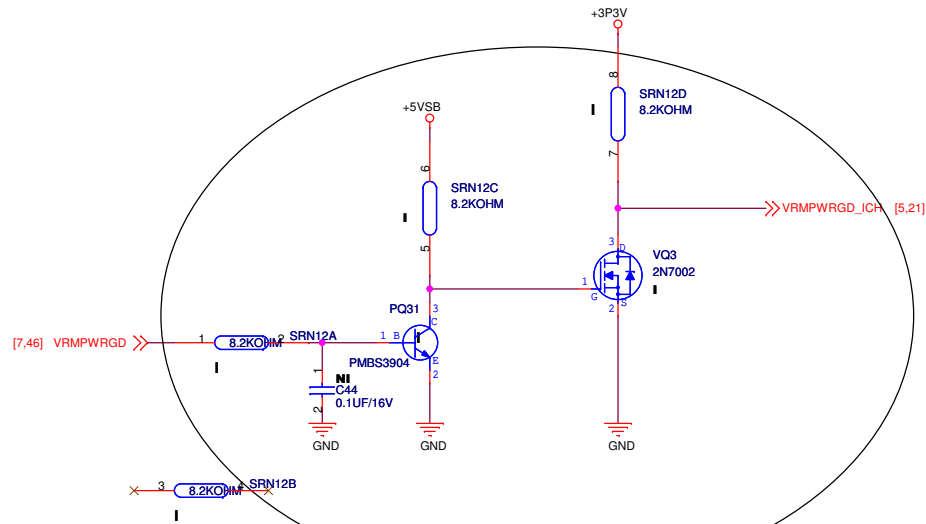
+5V_DUAL_USB_B.....3A

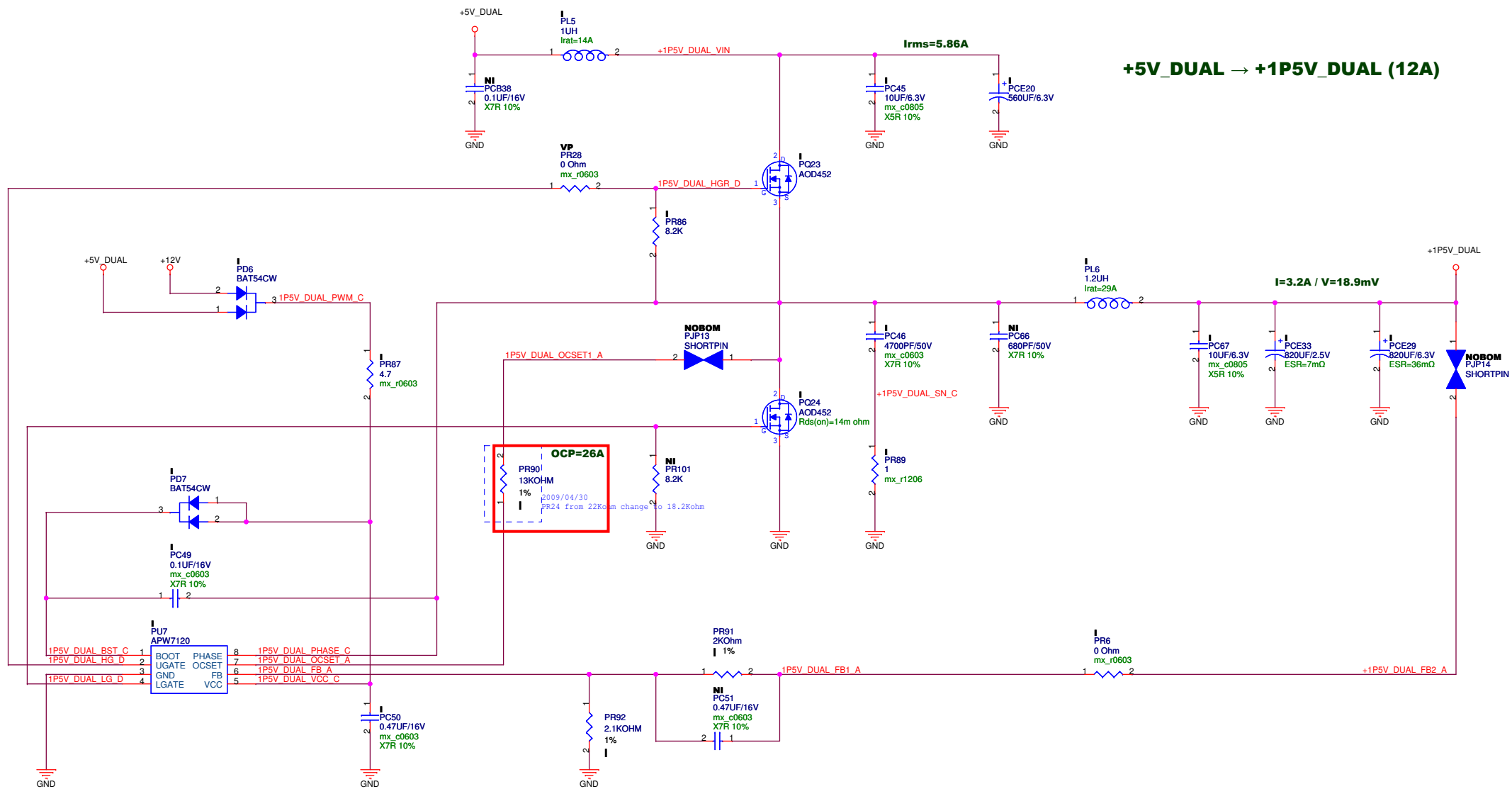


PSI CIRCUIT



VRMPWRGD CIRCUIT



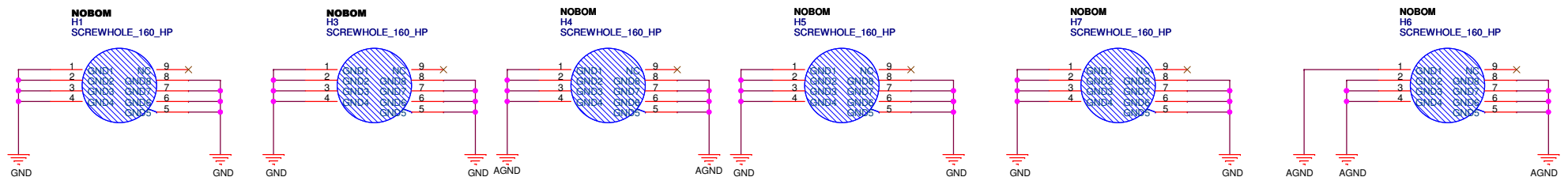
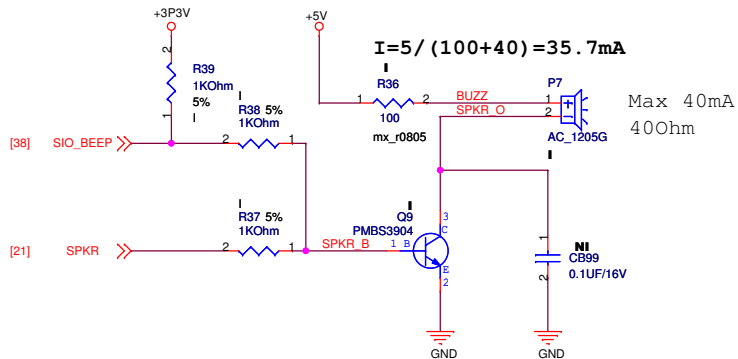


+5V_DUAL → +1P5V_DUAL (12A)

CLEAR CMOS



8/21 modify to 12



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : RTC / CMOS / SPKR

PEGATRON CORP.		Engineer: <i>Wayne Hsieh</i>	
Size A3	Project Name IPM41-D3	Rev 1.00G	
Date: Thursday, July 09, 2009		Sheet 55 of 55	